Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.976
High Speed Communication Circuits and Systems
Spring 2003

Homework #5: Voltage Controlled Oscillators

Reading: Chapters 16 and 17 of Thomas H. Lee's book. Chapter 7 of Behzad Razavi's book.

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1. The following is based on Problem 4 in Chapter 16 of Thomas Lee's book, and considers the differential CMOS VCO shown in Figure 1. Assume the bulk nodes of the PMOS and NMOS are tied to their respective source nodes.

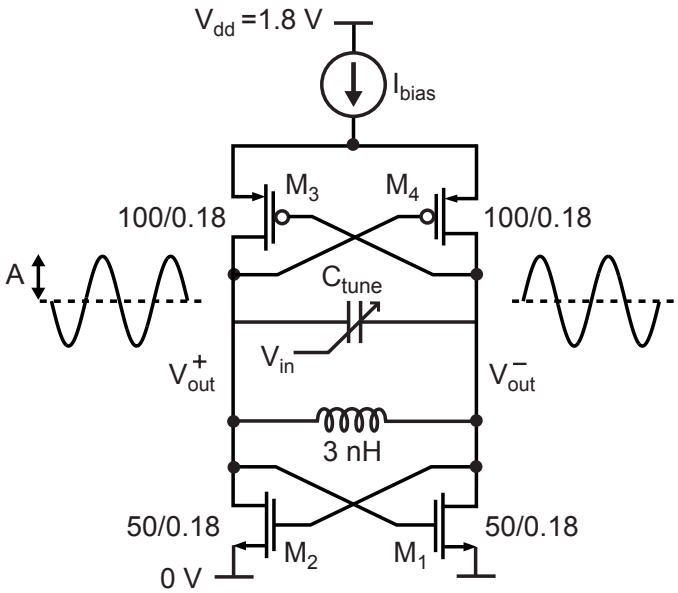

Figure 1: Differential CMOS LC Oscillator.

(a) Neglecting transistor capacitances, calculate the oscillation frequency assuming C_{tune} has been adjusted to a value of 2 pF.

(b) Using Hspice and the mos018.mod MOS models, determine the minimum value of bias current, I_{bias}, such that sustained oscillation can be achieved in the tank. Assume an inductor with Q=10 at the oscillation frequency is the only source of loss in the tank.

(c) Using minimum I_{bias}, extract the transistor capacitances and determine the new oscillation frequency. By how much did the frequency shift from that found in part (a)?

(d) Calculate the oscillation amplitude, A, as a function of I_{bias} under the assumption that the current waveforms through the transistors are square waves, and that the oscillator is in the current-limited regime.

(e) Assuming that the tank abruptly shifts to the voltage-limited regime when the oscillator amplitude equals half the supply voltage (V_{dd}), determine the value of I_{bias} for which the phase noise of the oscillator will be minimized.

(f) Is it possible to use a series tank instead of a parallel tank here? Explain.

2. The following combines Problem 2 and 8 in Chapter 16 and 17, respectively, of Thomas Lee's book. Here we examine the Colpitts oscillator shown in Figure 2. Use the 0.18u Hspice model file provided on Athena in the file /mit/6.976/Models/0.18u/mos018.mod for your MOS model.

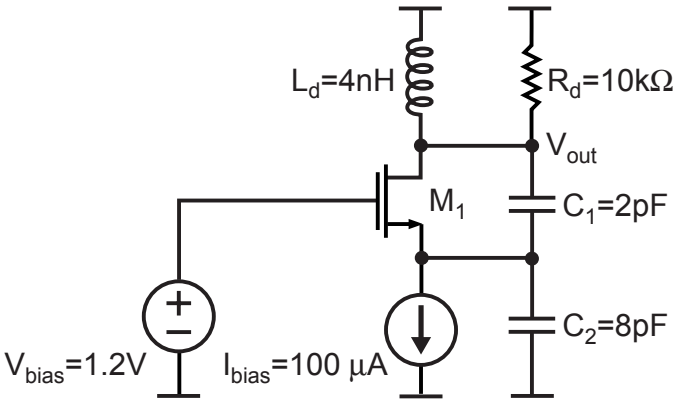

Figure 2: CMOS Colpitts oscillator.

(a) Neglecting transistor capacitances and r_o, calculate the minimum W/L ratio necessary for a startup gain of 2 under the assumption that the device obeys the square law for its V_{gs} to I_d curve. What should L be set to? Explain.

(b) Would there be an advantage to setting the startup gain to a value just slightly higher than 1? If so, why not do so?

(c) Given the same conditions as part (a), find the minimum W using Hspice. Use the L value previously selected in (a). (Suggestion: If you encounter problems passing parameters from Cadence to the Spice netlist, consider modifying your Spice netlist (i.e., *test.sp*) file after running *hspc* and then running *hspice*.)

(d) Suppose that the tail current source of the oscillator, I_{bias} is replaced by a 1.3 kΩ resistor and the device size chosen to achieve a startup gain of 2. For simplicity, assume that the transistor can be approximated by its small signal equivalent model, and that the oscillator output amplitude is 0.9 V.

i. Model the noise introduced by the 1.3 kΩ resistor as an equivalent noise current source in parallel with the inductor.

ii. Ignoring all other noise sources, calculate the phase noise of the oscillator due to this resistor's noise. What's the phase noise (dBc/Hz) at 1MHz offset? (Let T=290 K)

3. The following problem focuses on analysis of the linearized oscillator model shown in Figure 3. It is assumed, for simplicity, that both of the current noise sources are white, and that the comparator is ideal (i.e., has infinite slope at its transitions, and no internal noise sources).

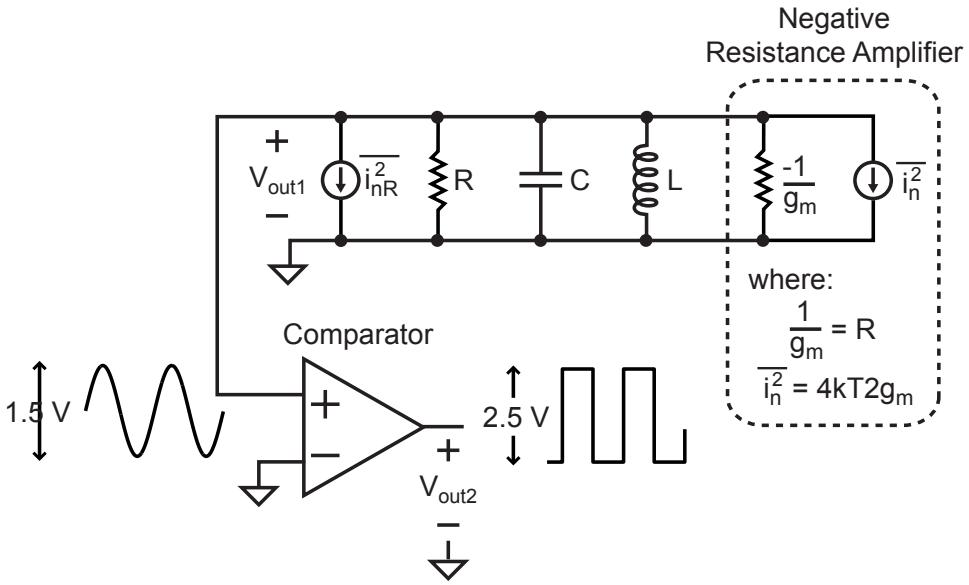

Figure 3: Linearized model of an oscillator feeding into a comparator.

(a) How does the noise of the tank effective resistance, R, compare to that of the amplifier? Do you think this observation will hold over a wide range of LC oscillators?

(b) How does the phase noise of V_{out1} compare to the phase noise of V_{out2}?

(c) Derive an expression for the phase noise spectrum of V_{out1} using Leeson's approach.

(d) Re-derive the expression for the phase noise spectrum of V_{out1} using the LTV (linear, time-varying) analysis method described in Chapter 17 of Thomas Lee's book. In your calculation, assume that the oscillation waveform and ISF are sinusoidal and that the noise sources are stationary.

(e) Compare your answers and provide an explicit expression for F, the Leeson fitting parameter, based on its use in Equation 13 of Chapter 17, for the linearized oscillator model.

4. This problem introduces you to spur level calculations and simulation.

   Consider a VCO with a spurious signal entering at its input as depicted in Figure 4. The voltage, v_{in}, to frequency output, f_{out}, characteristic of the VCO is assumed to be:

$$f_{out} = (K_v v_{in} + f_o)Hz, \text{ where } K_v = 10 \text{ MHz/V}, \ f_o = 100 \text{ MHz}.$$

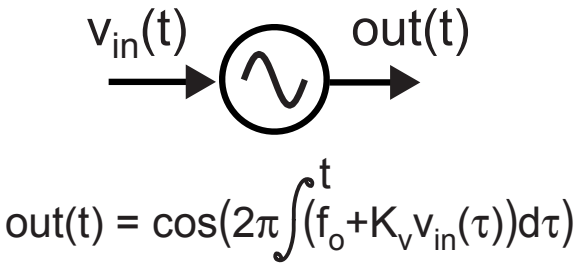

Figure 4: VCO block and associated equation.

   (a) Assuming that $v_{in} = A\sin(2\pi f_{spur}t)$, derive an expression for the magnitude (in dBc) of the spurs that result at the output of the VCO.

   (b) Suppose v_{in} were changed to $v_{in} = A\sin(2\pi f_{spur}t) + V_B$, where V_B is a constant bias voltage. Does the value of V_B have any effect on the magnitude (in dBc) of the spurs?

   (c) Does the magnitude (in dBc) of the spurs depend on the value of the VCO output voltage swing?

   (d) Use CppSim to simulate the system depicted in Figure 4 with v_{in} specified as in part (b), where $V_B = 0$. Set the simulation sample rate to 1 GHz and the number of simulation samples to 10000, and configure the schematic according to the block diagram shown in Figure 5. Measure the spur levels in units of dBc by taking the fft (scaled in dB) of the sine wave output of the VCO and then comparing the spur to the carrier tone.

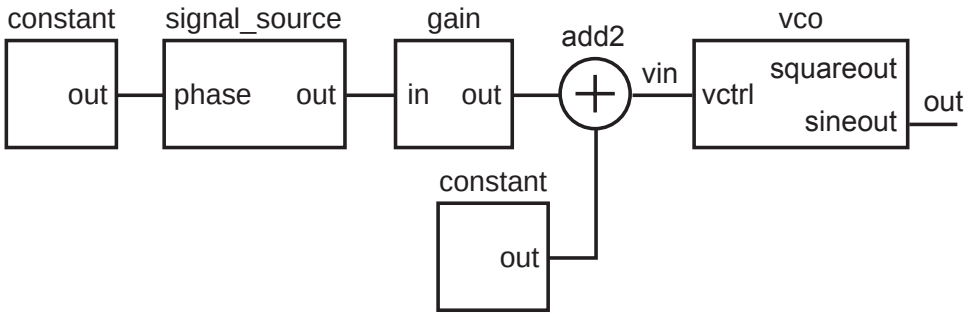

Figure 5: CppSim block diagram of VCO spur simulation.

Use CppSim and Matlab to plot the resulting spur levels for three different values of A and f_o:

case (i)	A = 100e-6	f_{spur} = 1 MHz
case (ii)	A = 100e-6	f_{spur} = 100 kHz
case (iii)	A = 10e-3	f_{spur} = 1 MHz

Label the magnitude of the (fundamental) spurs in dBc directly on the plots.

(e) Using the equation you derived in part (a), calculate the theoretical spur magnitudes (in dBc) for each of the cases in part (d), and check that the answers agree with the results from the simulation.

(f) Why do you see harmonics of the spur tones in case (iii)?

(g) Given the input levels of noise specified in part (d), how would the spurious noise of the VCO be impacted by increasing the value of K_v? For the best noise performance, would you choose a high or low value of K_v? Are there any negative consequences of choosing that (high or low) value of K_v?

(h) Based on this exercise, do you think that it's easy or hard to design a synthesizer with spurious performance better than -70 dBc?