Microfabrication for MEMS: Part II

Carol Livermore

Massachusetts Institute of Technology

* **With thanks to Steve Senturia, from whose lecture notes some of these materials are adapted.**

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Outline

> **Substrates**

> **Lithography and patterning**

> **Doping**

> **Thin films**

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Silicon Wafers

- Silicon is a diamond-structure cubic crystal
- Comes with different amounts of either n-type or p-type doping

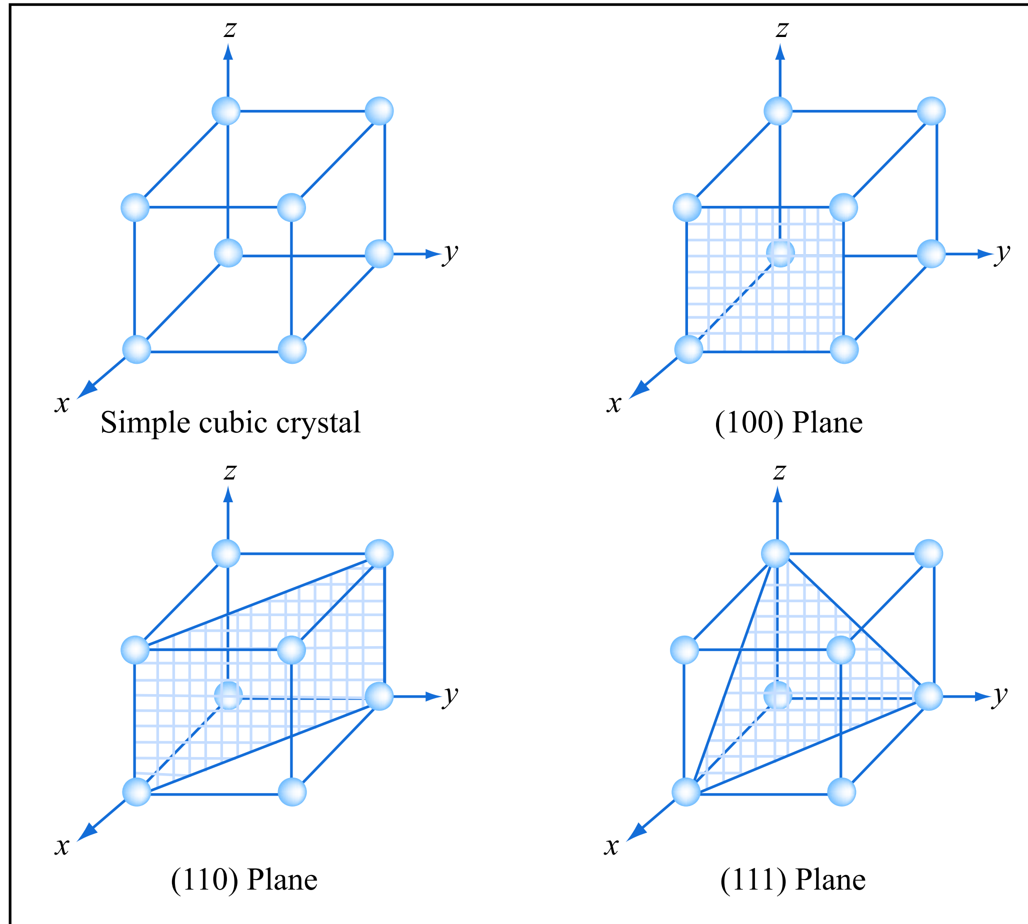


Image by MIT OpenCourseWare.

Adapted from Figure 3.1 in Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 31. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Notation

- A direction in crystal coordinates is denoted by square brackets, e.g. [100]
- The set of symmetrically equivalent directions is written with braces, e.g. <100>
- The plane perpendicular to a direction is denoted with parentheses, e.g. (100)
- The set of symmetrically equivalent planes is written with curly brackets, e.g. {100}

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Diamond Structure

> **The diamond structure is two face-centered cubic lattices shifted by ¼ of the body diagonal. There are four silicon atoms per cubic unit cell.**

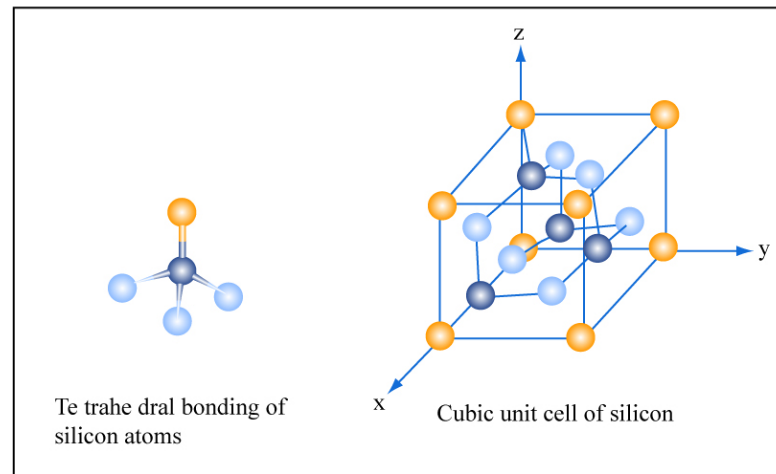


Image by MIT OpenCourseWare.

Adapted from Figure 3.2 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 32. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Wafer orientation

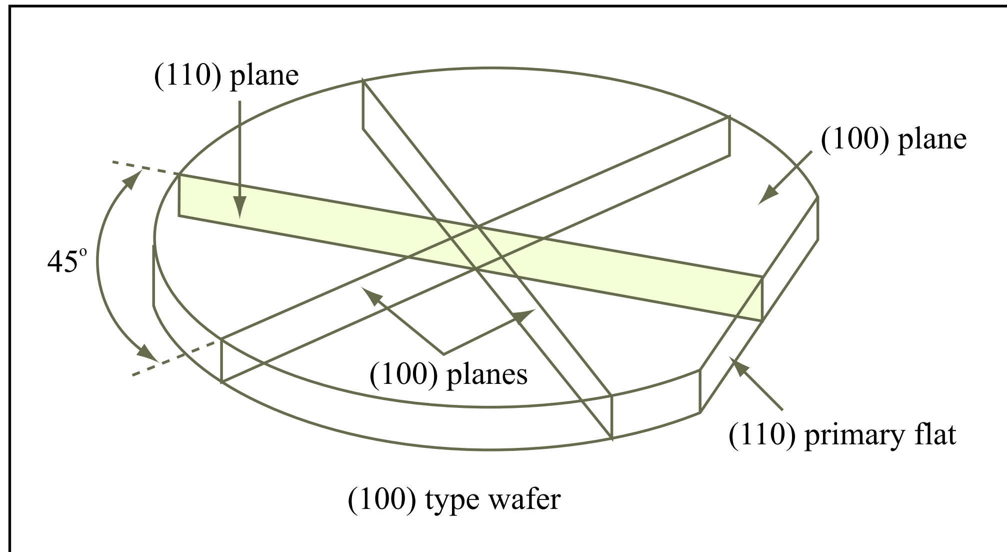


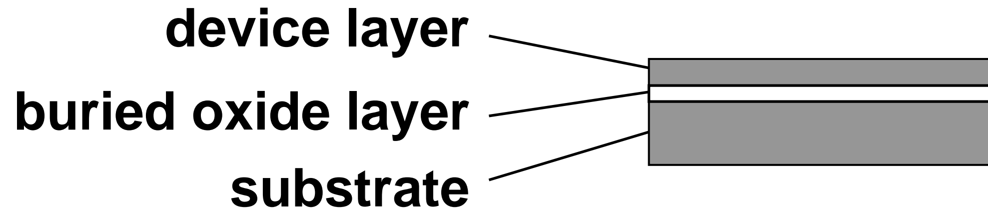
Image by MIT OpenCourseWare.
Adapted from: Maluf, Nadim. *An Introduction to Microelectromechanical Systems Engineering*.
Boston, MA: Artech House, 2000. ISBN: 9780890065815.

Picture from N. Maluf, An Introduction to Microelectromechanical Systems Engineering

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Other substrates

> Silicon wafers with embedded layers, such as silicon-on-insulator (SOI) wafers



- Initial purpose: build IC's on device layer, and buried oxide minimizes stray capacitance to substrate
- Common MEMS purpose: bulk micromachine top layer into moveable structures with well-controlled thickness
- $$$$

> Quartz wafers

- Single crystal
- Fused quartz – amorphous quartz wafers

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Other substrates

- Glass (cheap, high impurity content)
  - Inexpensive base for soft lithography
  - Transparent for optical access
  - Can be very strongly attached to silicon wafers via anodic bonding
- Compound semiconductors (III-V's, II-VI's)
  - Optical applications
- Sapphire
  - Strong, wear resistant, transparent, insulating substrate
  - Compatible with CMOS (so transparent CMOS MEMS)
  - Expensive, hard to etch

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Substrate summary

Substrate	Front end compatible	Back end compatible	Everything else compatible
Silicon	yes +	yes	yes, but only use if needed
Silicon on insulator (SOI)	yes +	yes	yes, but only use if needed
Quartz	yes	yes	yes, but only use if needed
Glass (pyrex)	no	yes, sometimes	yes +
Compound semiconductor	no	yes	yes, but only use if needed
Sapphire	yes, but only use if needed	yes, but only use if needed	yes, but only use if needed

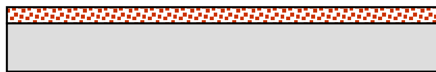
Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Outline

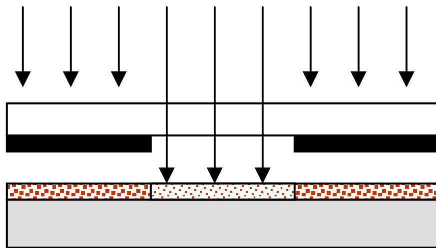
- Substrates
- **Lithography and patterning**
- Doping
- Thin films

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Optical Lithography



Spin-cast a photosensitive resist layer; bake out solvent



Collimated UV exposure through a mask; resist either cross-links or becomes soluble

positive

negative

Develop by dissolving the exposed/unexposed (positive/negative) resist; can now transfer pattern to substrate

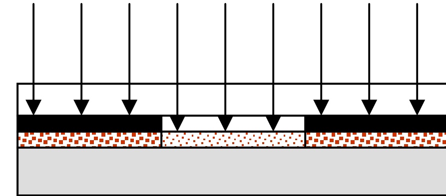
Alignment fiducials permit alignment of subsequent masks.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Methods of optical lithography I

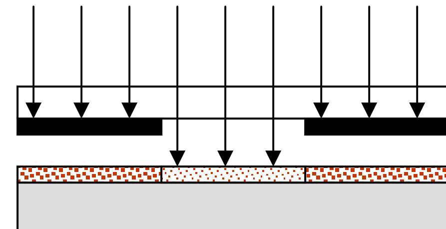
> Contact

- Mask touches wafer
- Inexpensive
- Contact degrades mask
- No die size limit
- Resolution: down to 1 micron nervously; down to several microns comfortably



> Proximity

- Mask of order 10 microns from wafer
- Inexpensive
- Less mask damage
- Diffraction means lower resolution
- No die size limit
- Resolution: down to several microns nervously, somewhat larger comfortably



Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Projection Lithography

- Projection lithography, especially when combined with an optical imaging system that reduces the image size, is used for high-resolution patterning (submicron to very submicron)
- Larger mask features, no contact with mask
- Wafer steppers expose one die at a time, assuring good focus and registration
- Something to consider: if your device needs fine features, a stepper may be required. But steppers have limits on die size of about 1 cm.

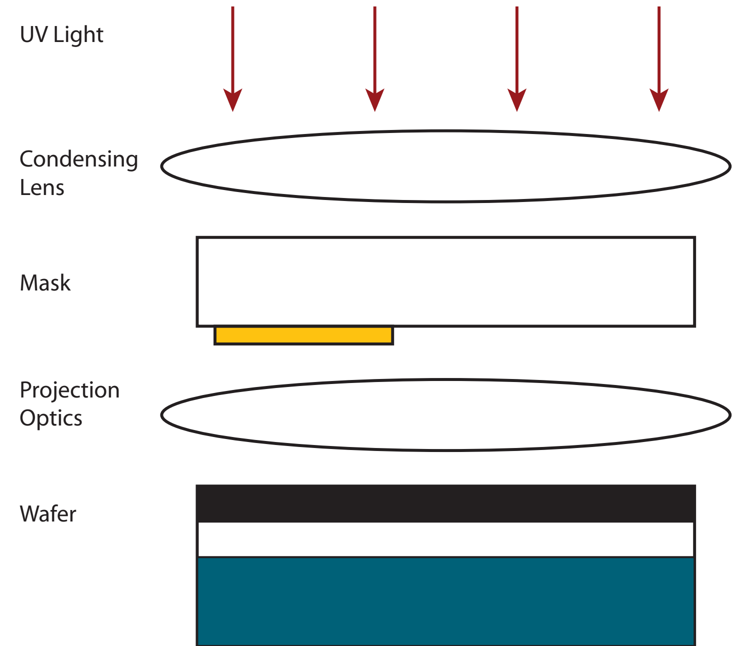


Image by MIT OpenCourseWare.
Adapted from Figure 3.15 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 53.
ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

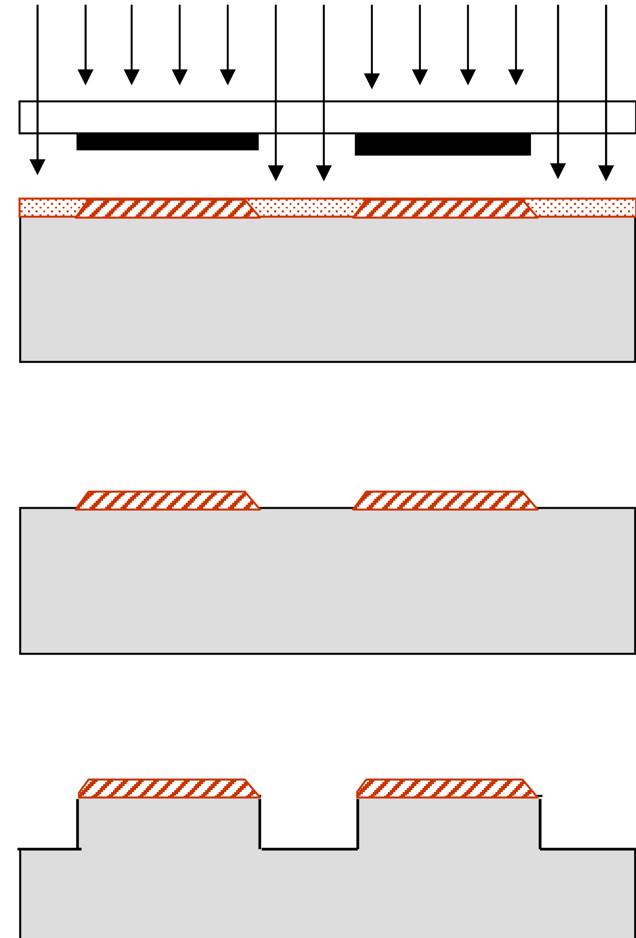
Mask making

- Highest quality – chromium on fused quartz written with an electron beam exposing an electron-beam resist (PMMA)
  - Also very high quality: laser-writing
- Photographic emulsion on fused quartz exposed with UV light flashes through a programmable aperture
- Patterns printed from an AutoCAD file on transparencies with a very-high-resolution printer – low resolution, but cheap and fast

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Positive thin resist

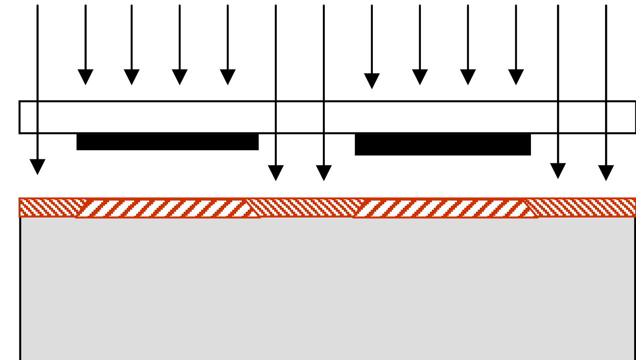
- Spin cast
- Thickness of order 1 micron
- Developer removes exposed resist
- Creates sloped profile at resist edge
- Some applications
  - Wet etching
  - Shallow dry etching
- Front end standard

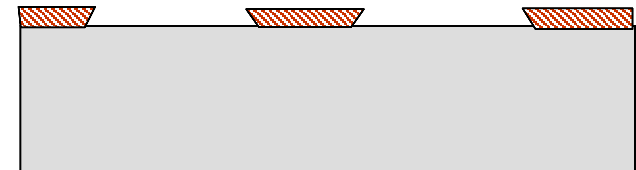


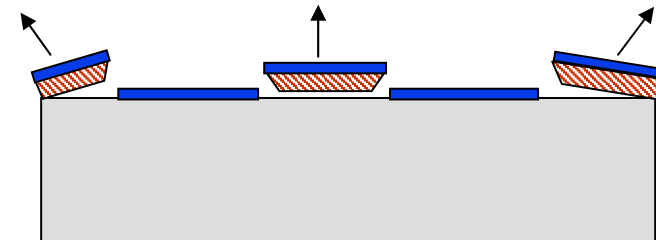
Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Negative/image reversal photoresists

- Spin cast
- Thickness of order 1 micron
- Developer removes unexposed resist
- Creates a re-entrant profile
- Typical application: liftoff processes (in acetone), often seen in back end processing
- Rule of thumb: resist thickness should be 3x thickness of layer to be lifted off
- Not a standard front end material, but not inherently incompatible with it



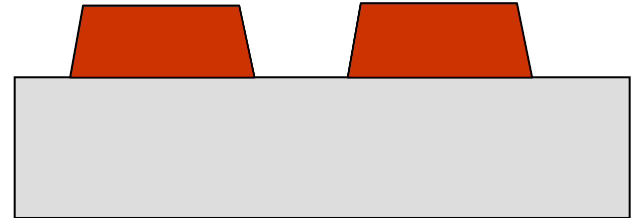


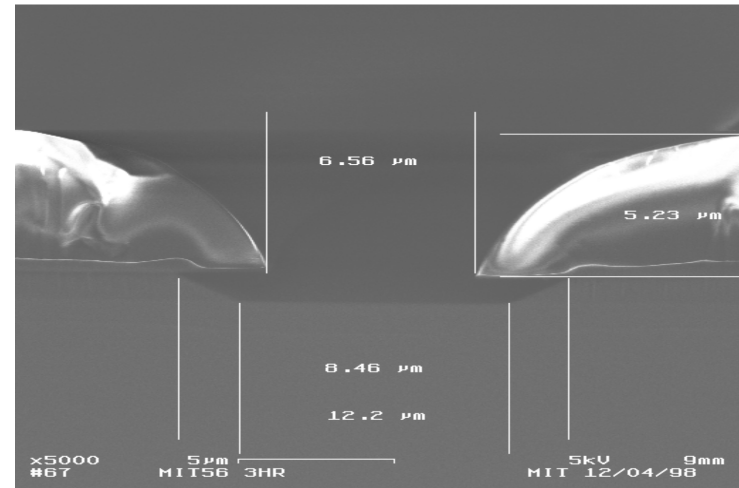


Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Positive thick photoresist

- Spin cast
- Thicknesses of order 10 microns
- Sloped profiles
  - Slope somewhat controllable through process conditions
- Some planarizing capability
- Typical applications:
  - Prolonged or low selectivity dry etch
  - Deep reactive ion etch
  - Masking any etch over topography
- Not a standard front end material, but not inherently incompatible with it





Courtesy of Reza Ghodssi. Used with permission.

5 µm thick

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Double-sided aligned lithography

- Goal: align features on the back of the wafer to features on the front
  - Common requirement in bulk micromachining
  - Not a standard IC capability
  - Functionality more common as market grows
- What you need:
  - Double side polished wafer
  - Double sided alignment tool
    - IR alignment, registration to global fiducials in the tool, through holes, etc.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Special purpose lithographic techniques I

> X-ray lithography
- One application: making molds for LIGA
- Requires an x-ray source and x-ray mask

> Electron beam lithography
- High resolution (tens of nanometers)
- NEMS (NanoElectroMechanical Systems)
- A slow, serial process

> Lithographic techniques that are rarely seen in front end processing

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Special purpose lithographic techniques II

> Shadow masking
- Direct evaporation or sputtering through physical holes in a shadow mask (think stencils)
- Back end/everything else process
- "Last ditch" technique for patterning surfaces that cannot be coated with resist (large topography, fragile features)

> "Soft lithography" (Whitesides, Harvard)
- Using polydimethylsiloxane (PDMS, a rubber material) as a physical mold to replicate structures
- Advantages:
  - » Patterning curved surfaces
  - » Rapid, inexpensive fabrication
- A set of everything else processes
- More on this later

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Very thick photoresists

> SU-8 epoxy
  - Spin cast
  - Negative resist, optical exposure
  - Can planarize extreme topographies
  - Can be structural, not easily dissolved

> Polyimide
  - Spin cast
  - Can planarize topographies
  - Humidity sensitive

> Classified as “everything else”

SU-8 epoxy photograph.

Image removed due to copyright restrictions.

500 micrometer SU-8 epoxy within deep silicon trench.

Image removed due to copyright restrictions.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Details that matter for lithographic patterning

> Existing topography: if your existing feature heights are comparable to or greater than the thickness of the resist that you are putting down, you will not have good coverage

- Incompletely covered sidewalls, holes full of resist, resist that never enters a hole at all
- Solutions: eliminate the topography, thicker resist, alternate coating technology (spray on, electrophoretic photoresist?), use of a previously patterned hard mask instead of a resist mask

> Patterned resist does not have a square profile – can affect the topography of whatever you pattern with the resist

> Resist adhesion

- If the surface of the wafer is hydrophilic (like SiO_2), the resist might peel during subsequent wet processing steps
- Surface preparation is key (e.g. dehydration bake and HMDS coating to render surface hydrophobic)

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Cleaning!

> **When we say (for example) that positive thin resist is compatible with front end processing, we do not mean that you can have resist on your wafer during most front end processes!**

> **Must remove resist and clean wafer thoroughly before high temperature processes**

> **Always include cleaning in process flows, starting at the crayon engineering level**

> **Resist removal techniques:**

- **O_2 plasma ash**
- **Chemical removal of organics: piranha clean (3:1 H_2SO_4:$H_2 0_2$) or Nanostrip (a weaker version of piranha)**
- **Solvents (acetone)**

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

More cleaning!

> Additional cleans typically needed at specified points in the flow

> Example: RCA clean before very high temperature processing (as in furnace for front end processing)

- Step 1: Organic clean, 5:1:1 $H_2O:H_2O_2:NH_4OH$ at 75 - 80C
- Step 2: Thin oxide removal, 50:1 $H_2O:HF$
- Step 3: Metal/ionic contamination removal, 6:1:1 $H_2O:H_2O_2$: HCl at 75 – 80C

> Example: remove organics before moderately high temperature, fairly clean processing (upper part of back end processing)

- Piranha clean (3:1 $H_2SO_4:H_20_2$)

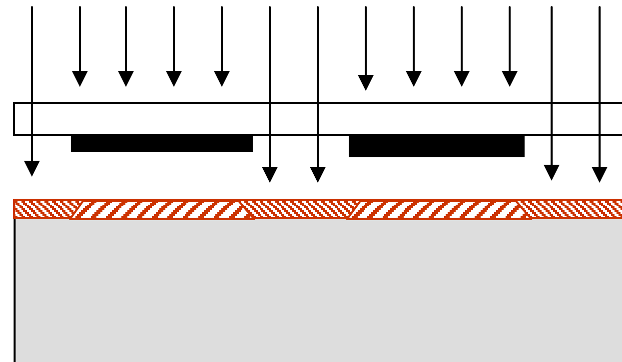
> Materials compatibility (what cleans your structures can tolerate) often determine what processes you can and can't use

> If you wait until the last minute to put cleans into your process flow, you will likely be redesigning your device and process at the last minute

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Another important detail: process bias

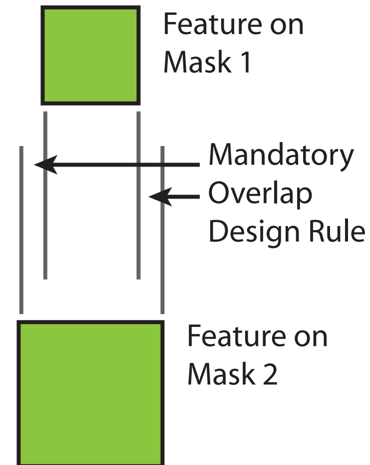
- The feature drawn on the mask is not the same size as the feature produced on the wafer
- Exposed area usually extends beyond clear area on mask
- Resist selection impacts process bias
  - Resist thickness
  - Resist tone

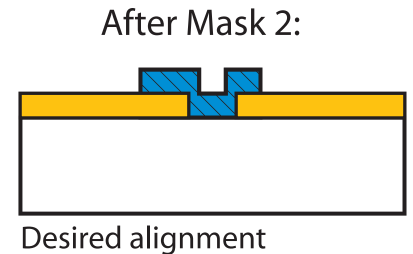


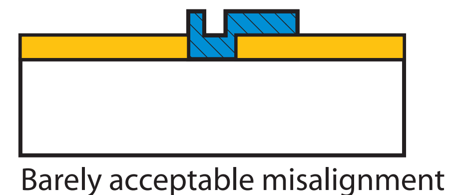
Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Design Rules

- **Alignment of one pattern to the next is critical to device fabrication**
- **Design rules are created to assure that fabrication tolerances do not destroy devices**







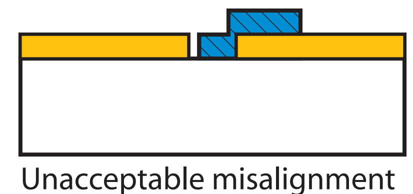


Image by MIT OpenCourseWare.
Adapted from Figure 3.16 in: Senturia, Stephen D. *Microsystem Design*. Norwell, MA: Kluwer Academic Publishers, 2001, p. 54. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Outline

- Substrates
- Lithography and patterning
- Doping
- Thin films

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Doping

- Doping is the introduction of a controlled amount of impurities to change the conductivity type and degree of a semiconductor
- In silicon, boron is a p-type dopant (creating holes), while phosphorus, arsenic, and antimony are n-type dopants (creating conduction electrons)
- Some doping incorporated in initial silicon melt
- All modern thin film doping is done with ion implanation
- Doping doesn’t add a new thin film, but it modifies the properties of a thin film at the surface of existing material

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Ion implantation

- A high-voltage accelerator is used to shoot ions at the wafer.
- The beam must be rastered and the wafer must be rotated to achieve uniform dose
- Usually a thin protective layer, such as oxide, is used to prevent sputtering of the surface and to reduce channeling
- The depth of the implant dose depends on energy
- Activation anneal after implantation allows dopants to reach proper positions in crystal

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Effective range

> **The effective range measures the location of the peak concentration of an implanted species.**

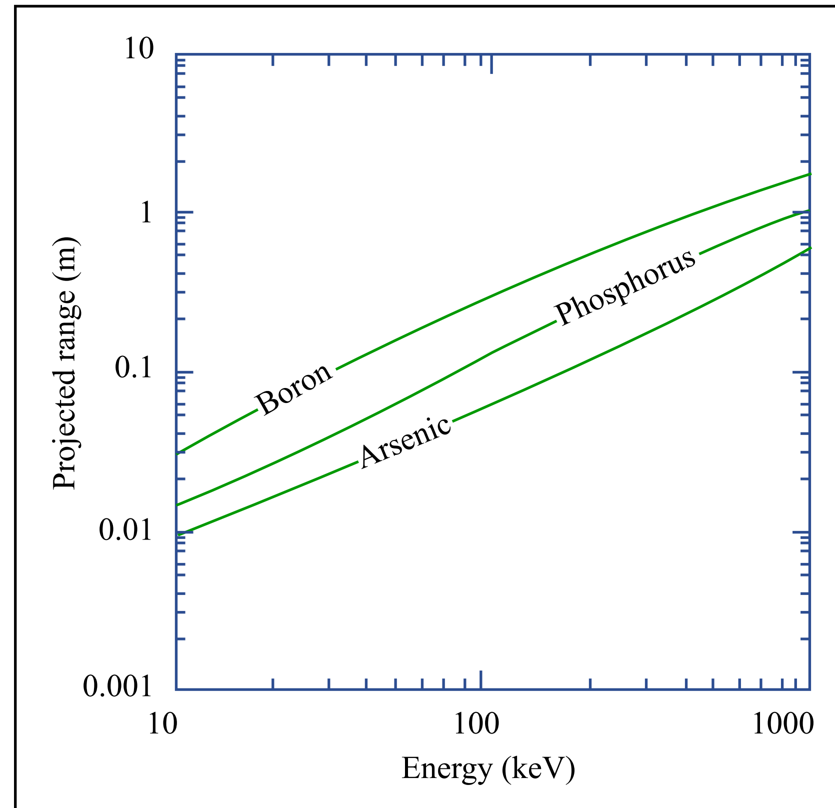


Image by MIT OpenCourseWare.

This image is for illustration purposes only; it should not be used for design calculations.
Adapted from Figure 3.6 in Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 39. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Masking of implants

> **Control of which regions of a wafer receive the implant is achieved with masking layers**

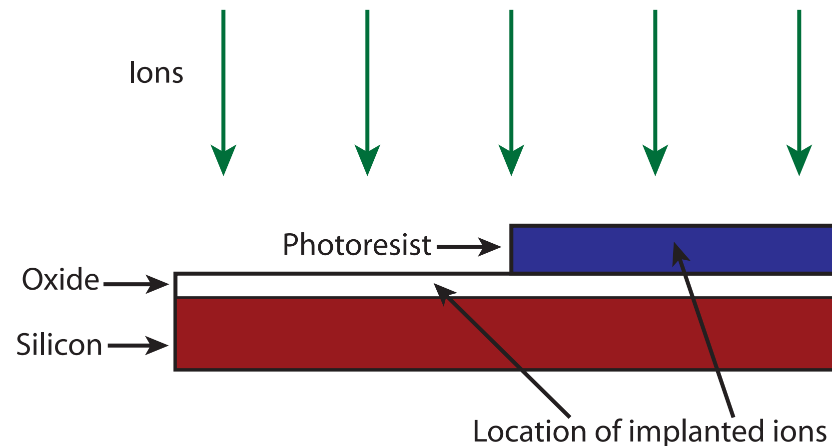


Image by MIT OpenCourseWare.
Adapted from Figure 3.7 in: Senturia, Stephen D. *Microsystem Design.* Boston, MA: Kluwer Academic Publishers, 2001, p. 39. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Diffusion

- After implantation, ions are driven deeper into the substrate by diffusion, a high-temperature process
- The junction depth is the point at which the implanted ion concentration is equal (but of opposite type) to the substrate doping

Implant dose

$$x_j = \sqrt{(4Dt)\ln\left(\frac{Q}{N_D\sqrt{\pi Dt}}\right)}$$

Background doping concentration

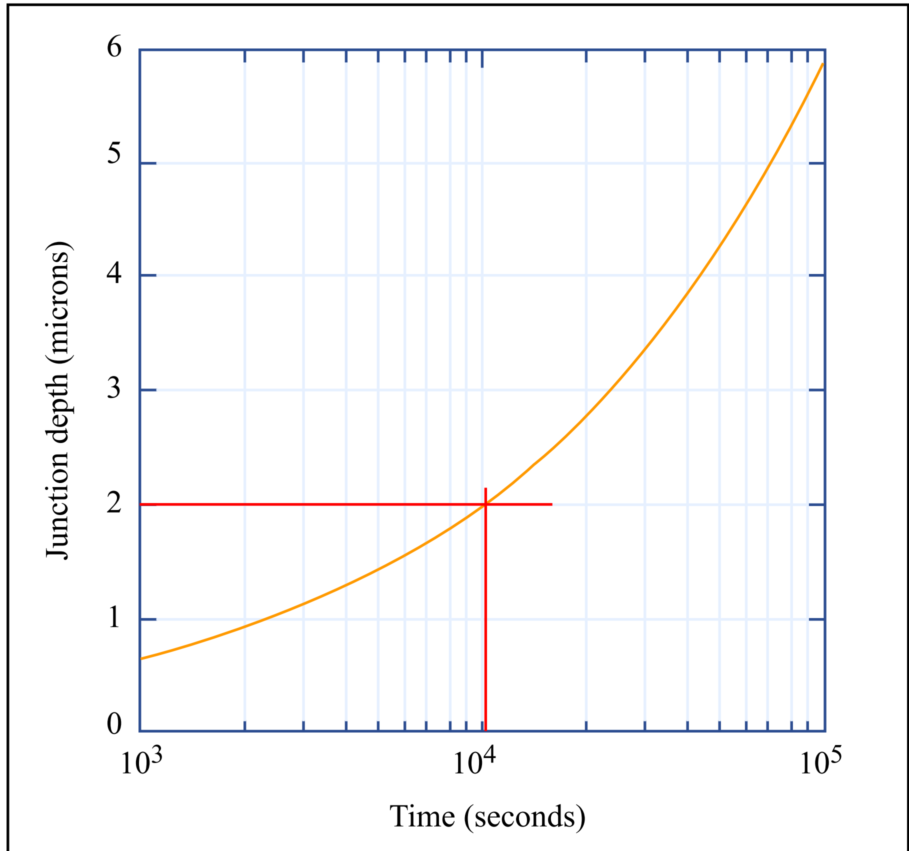


Image by MIT OpenCourseWare.

This image should not be used for design calculations. Adapted from Example 2.2 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 43. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Outline

- **Substrates**
- **Lithography and patterning**
- **Doping**
- **Thin films**

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Creating thin (and thick) films

> Many techniques to choose from

> Differences:

- Front or back end processes
- Quality of resulting films (electrical properties, etch selectivity, defects, residual stress)
- Conformality
- Deposition rate, cost

> Physical techniques

- Material is removed from a source, carried to the substrate, and dropped there

> Chemical techniques

- Reactants are transported to the substrate, a chemical reaction occurs, and the products deposit on the substrate to form the desired film

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

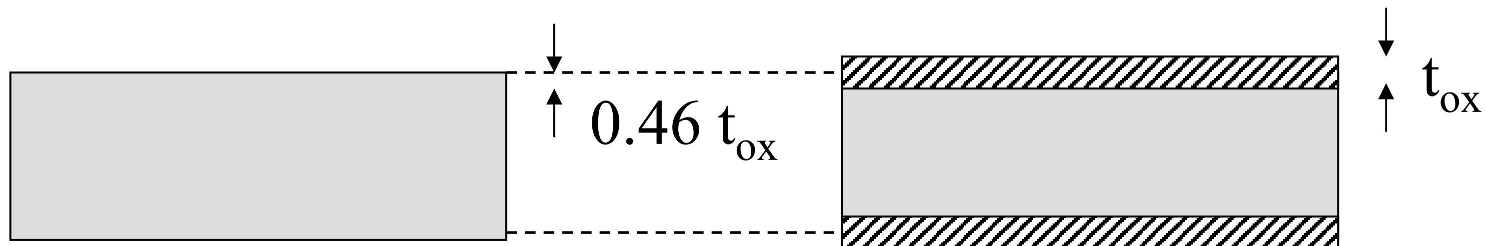
Taxonomy of deposition techniques

- Chemical
  - Thermal Oxidation
  - Chemical Vapor Deposition (CVD)
    - Low Pressure (LPCVD), Atmospheric Pressure (APCVD), Plasma Enhanced (PECVD)
  - Epitaxy
  - Electrodeposition (Electroplating)
- Physical
  - Physical Vapor Deposition (PVD)
    - Evaporation
    - Sputtering
  - Spin-casting

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Oxidation I

- Silicon forms a high quality, stable oxide
- How it works:
  - Oxygen diffuses through oxide to Si/oxide interface
  - $Si + O_2$ + high temperature (~1100 C) furnace → SiO_2
  - Some Si is consumed



- Rate determined by diffusion of oxygen through oxide
- Diffusion limits practical oxide thickness to < 2 μm
- A key front end process

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Oxidation II

> Dry oxidation (O_2)
  - High quality, slow oxidation rate, smaller maximum thickness (*i.e.* gate oxide)

> Wet oxidation (steam)
  - H_2 to speed the diffusion
  - Lower quality, faster oxidation rate

> The Deal-Grove model describes the kinetics of oxidation quite well for oxides greater in thickness than about 30 nm.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Deal-Grove Model

For oxides greater than about 30 nm thick:

$$x_{final} = 0.5\left[A_{DG}\left[\sqrt{1+\frac{4B_{DG}}{A_{DG}^2}\left(t+\tau_{DG}\right)}-1\right]\right]$$

where $$\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{B_{DG}/A_{DG}}$$

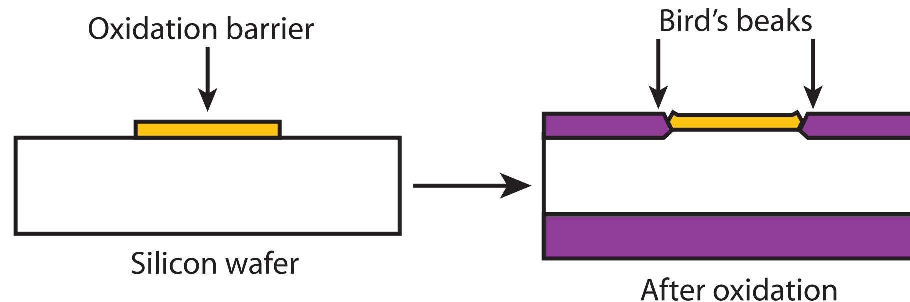
(Constants are given in the text; beware units of B_{DG}, μm²/hour)

Growth goes approximately as *t* for short times, and approximately as $\sqrt{t}$ for long times.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Local Oxidation

- Oxidation can be masked locally by an oxidation barrier, such as silicon nitride
- Oxide undercuts edge of mask layer to form a “bird’s beak”
- Oxidation followed by oxide etch can also be used to sharpen silicon features.



Senturia, Microsystem Design.

Image by MIT OpenCourseWare.
Adapted from Figure 3.5 in: Senturia, Stephen D. *Microsystem Design*.
Norwell, MA: Kluwer Academic Publishers, 2001, p. 37. ISBN: 9780792372462.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Chemical Vapor Deposition (CVD)

> How CVD works:
- Gaseous reactants, often at low pressure
- Long mean free path; reactants reach substrate
- Reactants react and deposit products on the substrate
- Unlike oxidation, does not consume substrate material

> Energy sources facilitate CVD reactions:
- High temperature, plasma, laser

> Processing temperatures vary widely

> Commonly deposited films: Oxide, silicon nitride, polysilicon

> CVD results depend on pressures, gas flows, temperature
- Film composition, uniformity, deposition rate, and electrical and mechanical characteristics can vary

> Near the boundary between front and back end, depending

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Some reasons to use CVD

> Oxide formation:
- To get a thicker layer than thermal oxidation can provide
- To create oxide on a wafer that can't withstand high temperatures (for example because of metal features)
- To create oxide on top of a material that is not silicon

> For film formation in general:
- To tailor the film properties (like film stress) by adjusting pressures, flow rates, external energy supply, ratios of different precursor gases (to adjust proportions of different materials in the final product)
- Conformality: (more or less) even coating on all surfaces

> Drawbacks
- Films deposited at low temperature are often lower quality than high temperature versions, and have less predictable properties
- Flammable, toxic, or corrosive source gases

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Thick Film Formation

- Chemical vapor deposition is a common MEMS tool for creating thick films on the wafer surface
  - In practice, film stress limits thickness (film delamination or cracking, or curvature of underlying structures)
  - Can deposit thick oxides; nitrides are still typically submicron
  - Must anneal deposited oxides for some applications – lose low stress property on anneal
- Example: PECVD deposition (350-400C) of 10 to 20 μm oxides

Image removed due to copyright restrictions.

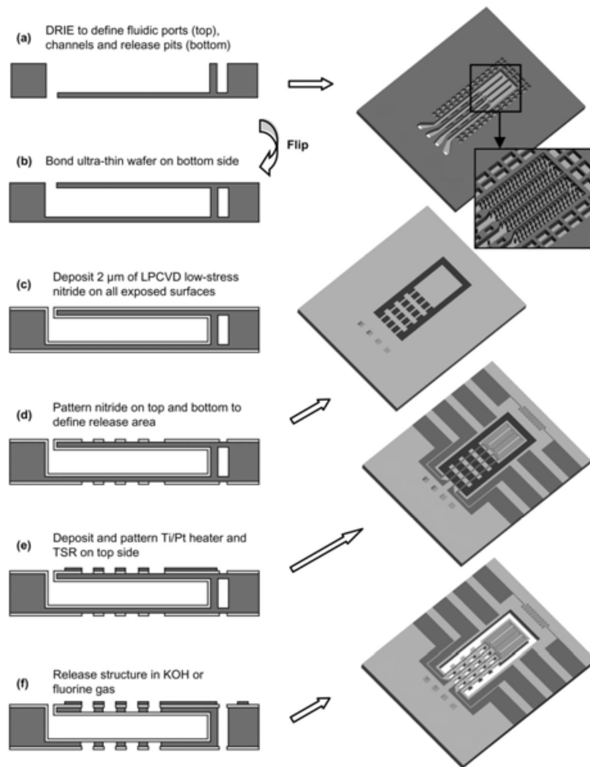
25 μm thick cracked oxide, X. Zhang et al., Hilton Head 2000

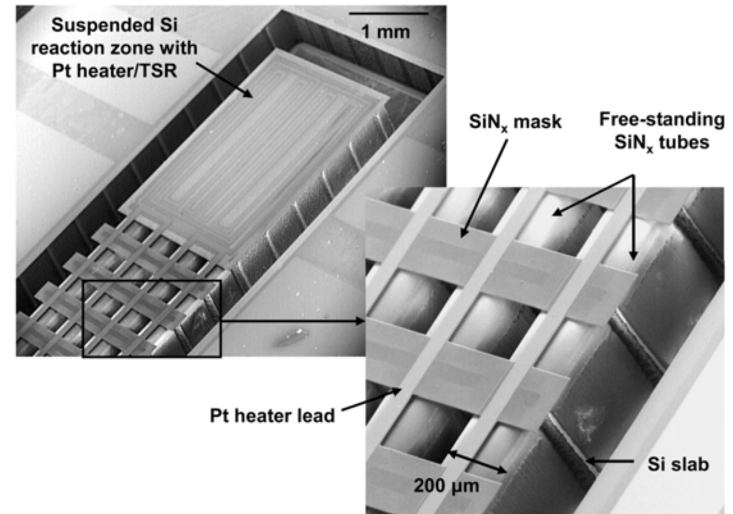
Image removed due to copyright restrictions.

18 μm thick oxide insulation for a microgenerator w/ Pt features

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

CVD enables conformal coating





MEMS-based fuel processor.

Figure 4 on p. 605 in: Arana, L.R., S. B. Schaevitz, A. J. Franz, M. A. Schmidt, K. F. Jensen, "A Microfabricated Suspended-tube Chemical Reactor for Thermally Efficient Fuel Processing." *Journal of Microelectromechanical Systems* 12, no. 5 (2003): 600-612. © 2003 IEEE.

Figure 5 on p. 606 in: Arana, L.R., S. B. Schaevitz, A. J. Franz, M. A. Schmidt, K. F. Jensen, "A Microfabricated Suspended-tube Chemical Reactor for Thermally Efficient Fuel Processing." *Journal of Microelectromechanical Systems* 12, no. 5 (2003): 600-612. © 2003 IEEE.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

LPCVD Polysilicon

- Amorphous at lower deposition temperatures and higher deposition rates
  - Typical temperature: ~ 590 C
- Polycrystalline at higher deposition temperatures and lower deposition rates
  - Typical temperature: ~ 625 C
- Grain size and structure depend on detailed deposition conditions
  - e.g. thicker films ⇒ larger grains
- Structure, electrical properties, and mechanical properties also vary with post-deposition thermal processing
  - Grain growth
  - Dopant activation or diffusion

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Polysilicon stress depends on deposition details

Image removed due to copyright restrictions.

Image removed due to copyright restrictions.

Kurt Petersen, Trans Sensory Devices

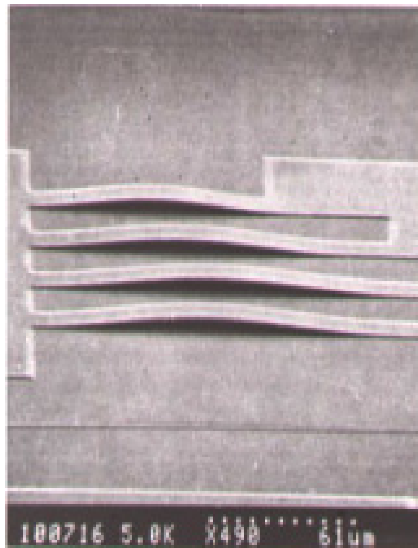


Image removed due to copyright restrictions.

Lober, Theresa Ann. "A Microfabricated Electrostatic Motor Design and Process." Masters thesis, Massachusetts Institute of Technology, 1988. 132 pages.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Epitaxy

> CVD deposition process in which atoms move to lattice sites, continuing the substrate's crystal structure
  - Homoepitaxy: same material, i.e. Si on Si
  - Heteroepitaxy: different materials, i.e. AlGaAs on GaAs

> How it happens
  - Slow deposition rate (enough time to find a lattice site)
  - High temperature (enough energy to move to a lattice site)

> Selective epitaxy is possible through masking

> Can grow a doped Si layer of known thickness

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

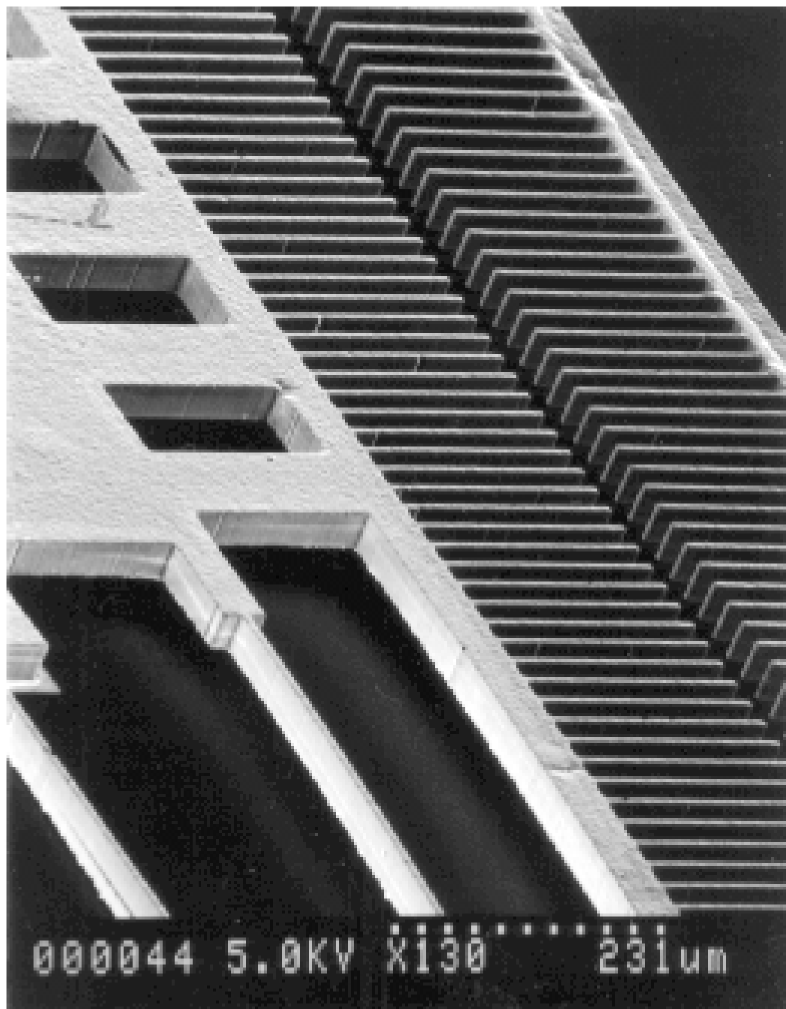
Electroplating: basics

> Pass a current through an aqueous metal solution
  - Anode is made of the metal that you want to deposit
  - Cathode is the conductive seed material on your wafer
  - Positive metal ions travel to the negatively charged cathode on your wafer and deposit there

> Preparing your wafer
  - If you want to plate metal in some places and not in others, you will need a patterned metal seed layer (and typically a “sticky” metal adhesion layer under that)
  - For very short features, just plate onto the seed layer
  - For taller features, need to plate into a mold
  - Molds can be photoresist, silicon, SU-8, etc., depending on the needs of your device

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Electroplating



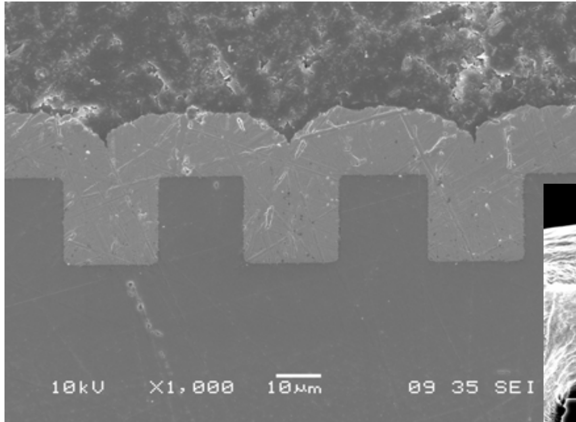
Electroplating for LIGA

40 µm thick films of nickel fabricated by electroplating into a mold

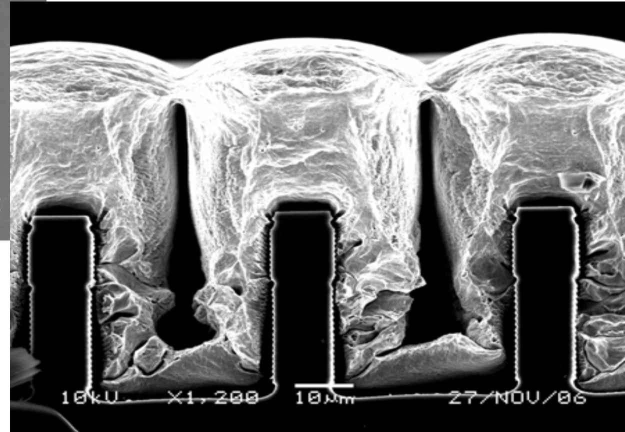
This picture belongs to Professor Reza Ghodssi (University of Maryland) and was published in the following reference: Ghodssi, R., D. J. Beebe, V. White, and D. D. Denton. "Development of a Tangential Tactor Using aLIGA/MEMS Linear Microactuator Technology." Proceedings of the 1996 ASME Winter Annual Mtg., Symposium on Micro-Mechanical Systems, Atlanta, Georgia, pp. 379-386, November 17-22, 1996.

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

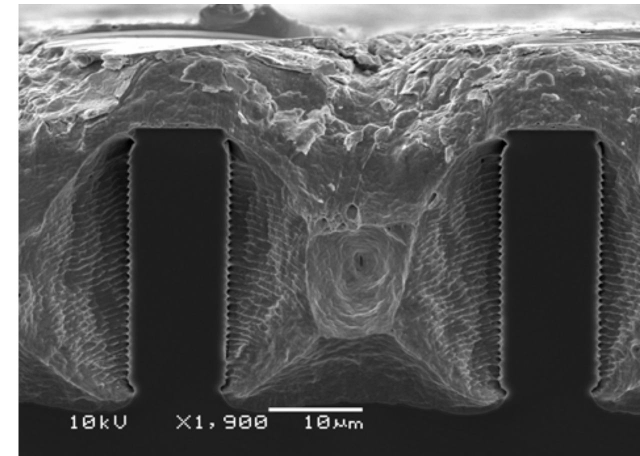
Electroplating realities



Test run w/ bump plating - perfect



Real device forms keyholes – different loading pattern



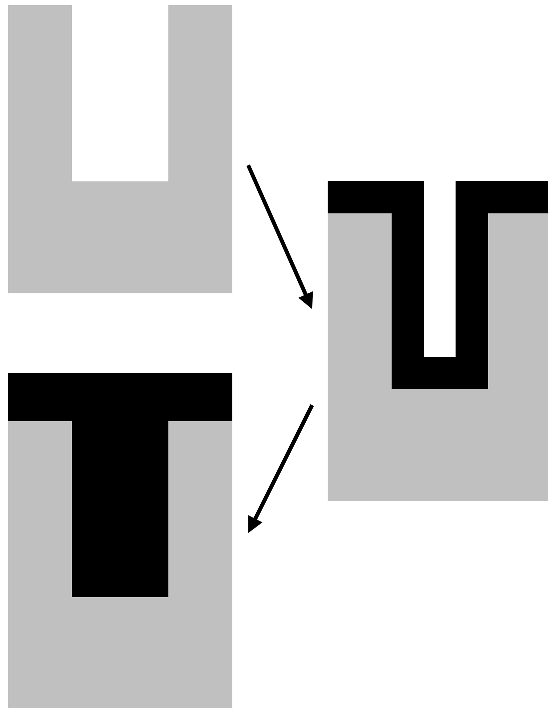
Courtesy of Dariusz Golda. Used with permission.

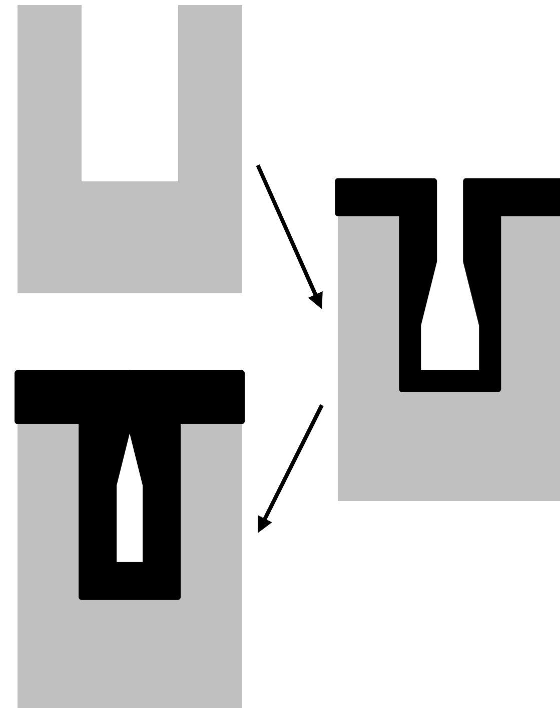
Solution: Cu damascene fill, with additives/agitation to promote fill at bottom

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Conformality and keyholes

- To lowest order, conformal films coat sidewalls and horizontal surfaces at the same rate.
- But high aspect ratio trenches are prone to keyholes (CVD, electroplating, etc.)





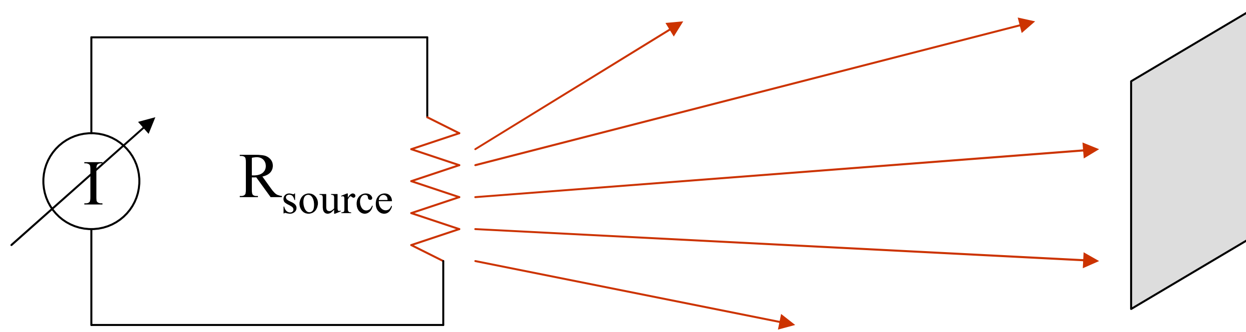
Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Physical Vapor Deposition (PVD)

- Remove material from a solid source
- Transport material to substrate
- Deposit material on substrate
- Differences among PVD techniques
  - How material is removed from source
  - Directionality when it arrives at substrate
  - Cleanliness of deposition
- A family of quick, low temperature processes
- All back end processes or worse

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

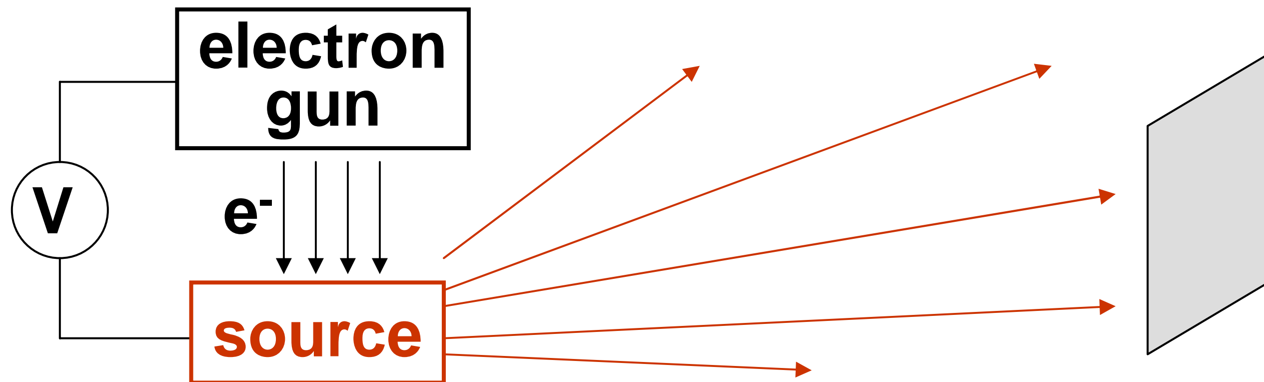
Thermal Evaporation



- Source is resistively heated in high vacuum
  - Typical source: metal
- Hot source atoms are emitted in all directions and stick where they land
- Substrate receives a directional flux of source material
  - Good for liftoff processes, otherwise poor conformality
- Possible contamination from generalized heating

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

E-beam Evaporation



> Electron beam heats source in high vacuum
- Typical source: metal

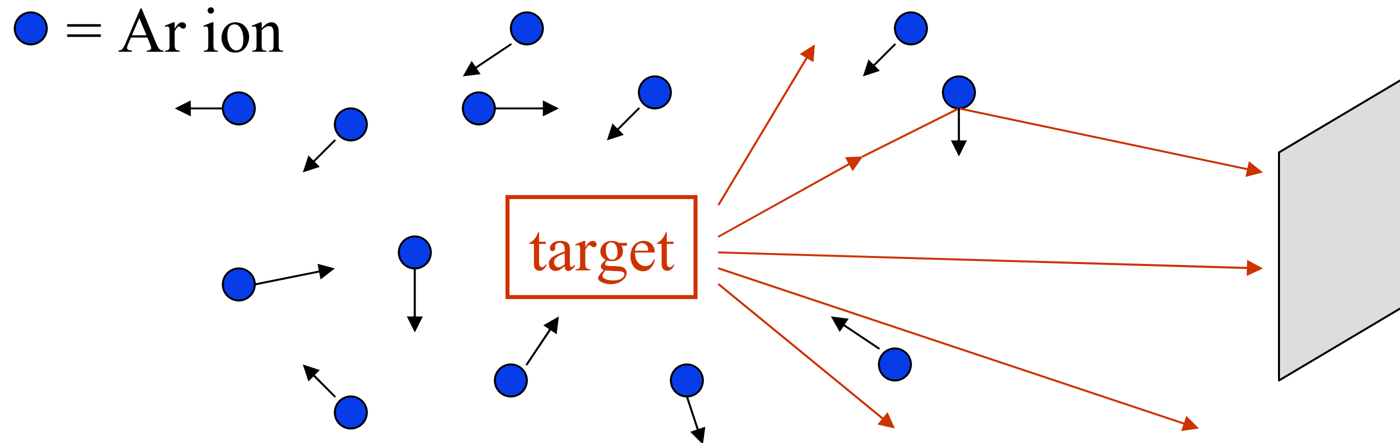
> Hot source atoms are emitted in all directions and stick where they land

> Substrate receives a directional flux of source material
- Good for liftoff processes, otherwise poor conformality

> Heating is less generalized → less contamination

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Sputtering



> Unreactive ions (i.e. Ar) knock material off a target by momentum transfer
> Targets: metals, dielectrics, piezoelectrics, etc.
> Different methods of obtaining energetic ions
  - Magnetron, plasma
> Low pressure, but not high vacuum
> Less directional and faster than evaporation

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Etching, liftoff, and adhesion layers

> Films are patterned differently depending on whether the material in question tends to react with other materials

> Materials that react (for example, aluminum):

- Deposit a blanket film (sputtering good for better conformality), do photolithography, and etch it into the desired shape

> Materials that don't react readily (for example, noble metals):

- Hard to etch: typically use liftoff instead
- Pattern resist, then deposit metal on top with a directional deposition tool
- Not very sticky: typically need an adhesion layer to stick the noble metal to what lies beneath
- Example: use a few hundred A thick layer of Cr or Ti to adhere Au to an underlying oxide (deposited without breaking vacuum between layers)

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Is this all you can do with deposited films?

- No!
- Spin-casting: put the stuff that you want to deposit in a liquid, spin it onto the surface like resist, and bake out the solvent (spin on glass, PZT piezoelectrics)
- Other forms of vapor deposition designed for a particular purpose (depositing the inert polymer parylene by vapor deposition followed by polymerization)
- Lamination of free-standing resist films onto surfaces
- Self assembled monolayers
- …

Cite as: Carol Livermore, course materials for 6.777J / 2.372J Design and Fabrication of Microelectromechanical Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].