6.776
High Speed Communication Circuits
Lecture 22

Noise in Integer-N and Fractional-N Frequency Synthesizers

Michael Perrott

Massachusetts Institute of Technology

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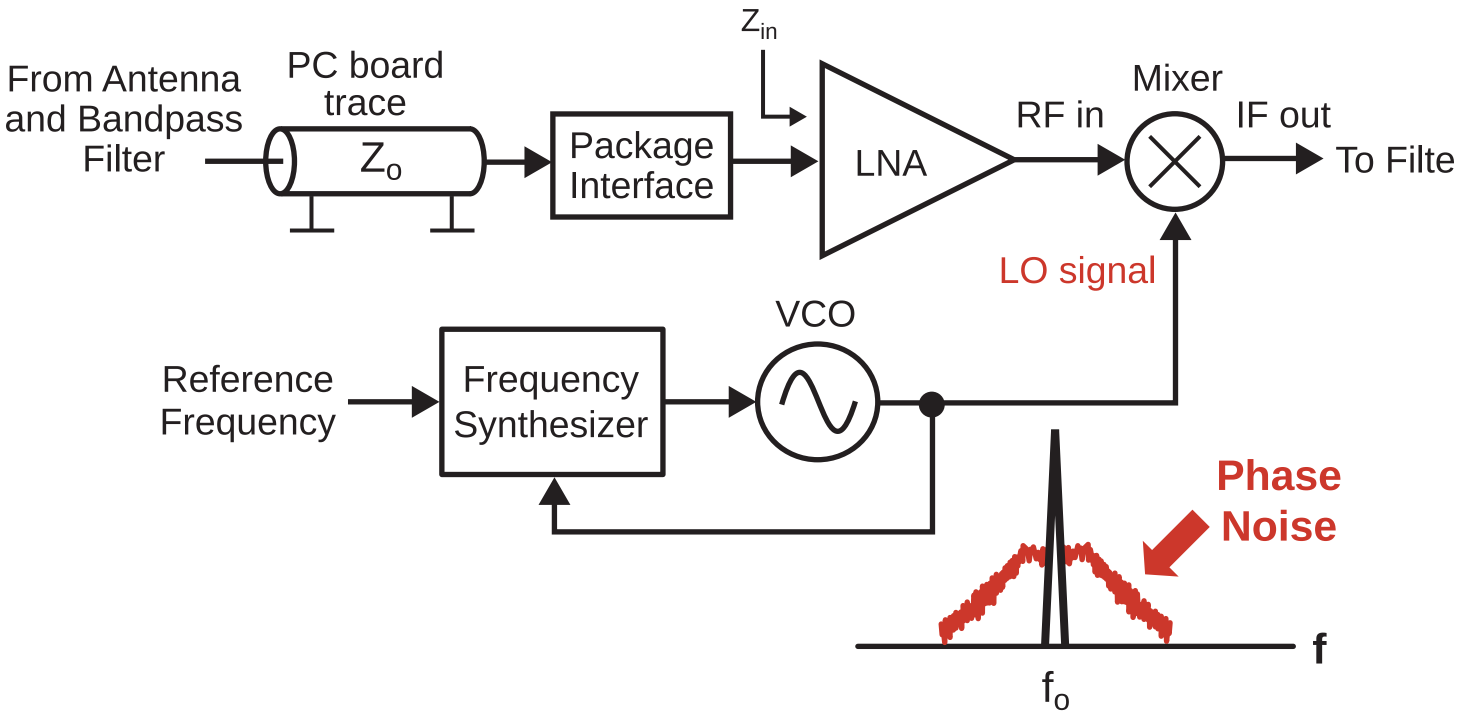
Outline of PLL Lectures

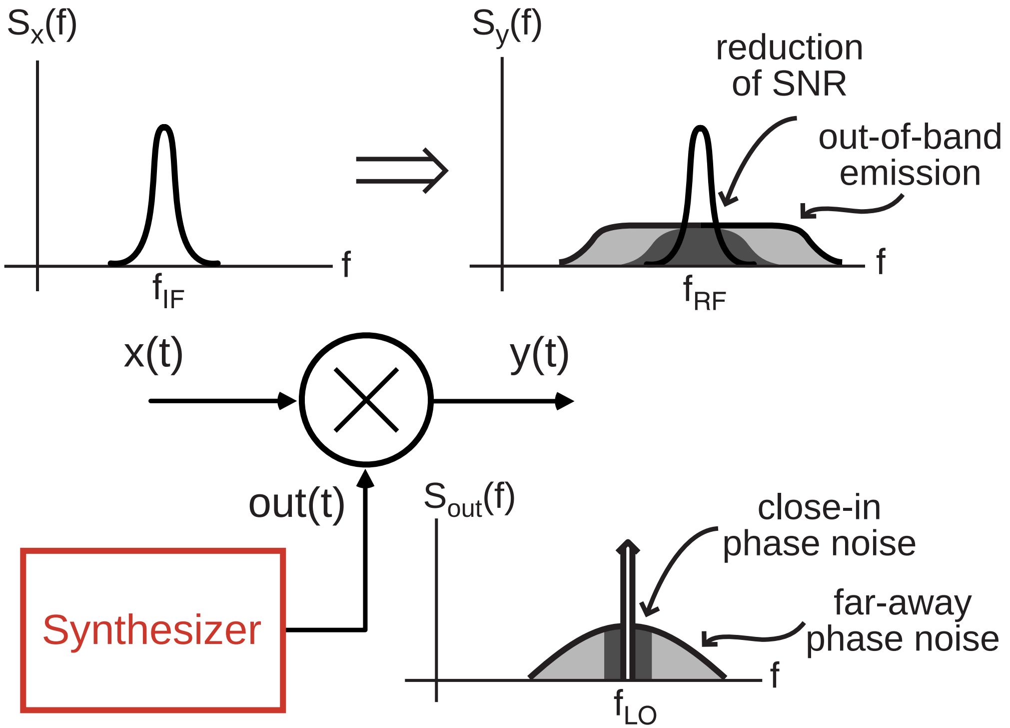
- Integer-N Synthesizers
  - Basic blocks, modeling, and design
  - Frequency detection, PLL Type
- Noise in Integer-N and Fractional-N Synthesizers
  - Noise analysis of integer-N structure
  - Sigma-Delta modulators applied to fractional-N structures
  - Noise analysis of fractional-N structure
- Design of Fractional-N Frequency Synthesizers and Bandwidth Extension Techniques
  - PLL Design Assistant Software
  - Quantization noise reduction for improved bandwidth and noise

Frequency Synthesizer Noise in Wireless Systems



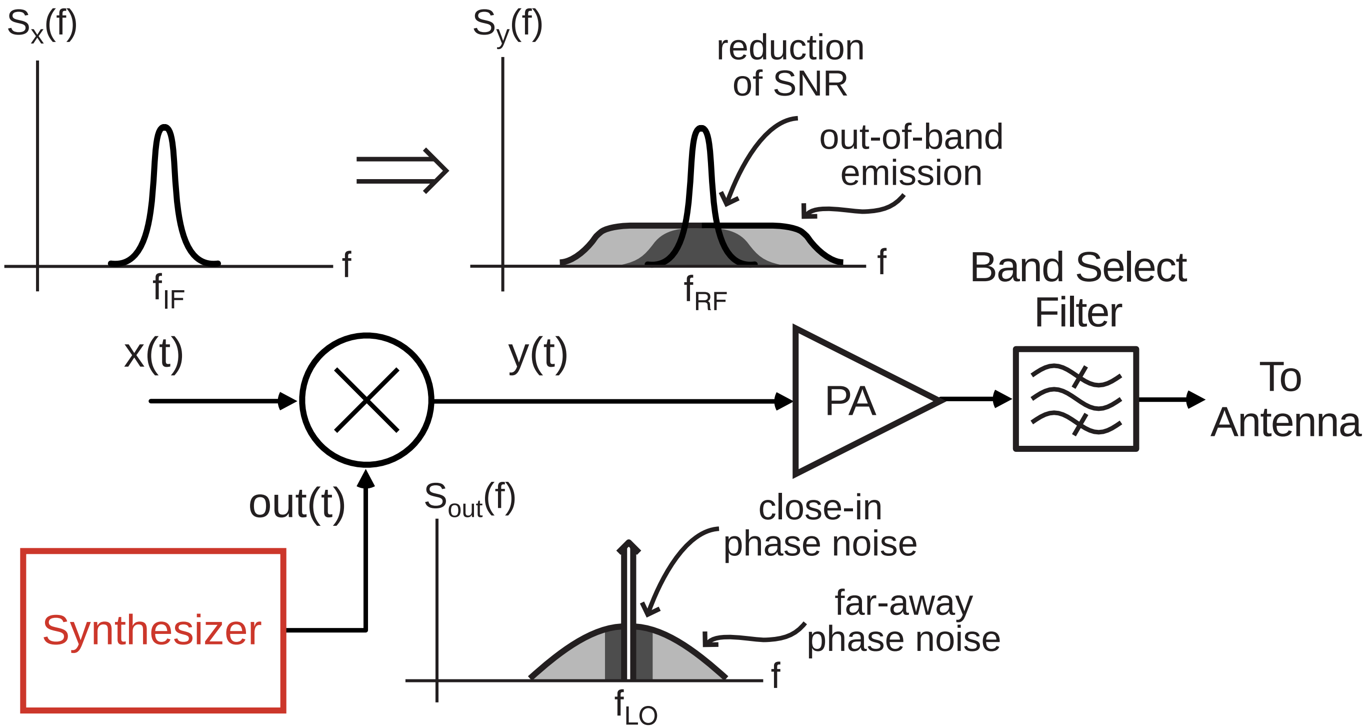
- **Synthesizer noise has a negative impact on system**
  - **Receiver – lower sensitivity, poorer blocking performance**
  - **Transmitter – increased spectral emissions (output spectrum must meet a mask requirement)**
- **Noise is characterized in frequency domain**

Impact of Synthesizer Noise on Transmitters



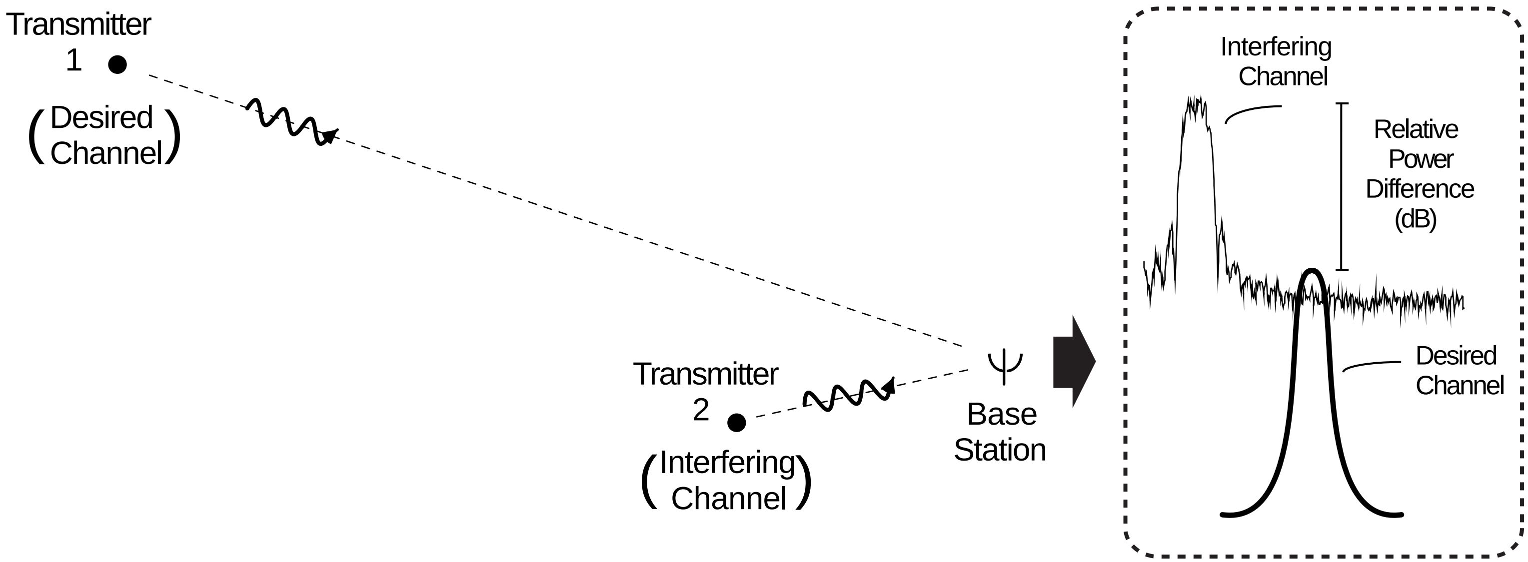
- **Synthesizer noise can be lumped into two categories**
  - **Close-in phase noise: reduces SNR of modulated signal**
  - **Far-away phase noise: creates spectral emissions outside the desired transmit channel**
    - This is the critical issue for transmitters

Impact of Remaining Portion of Transmitter



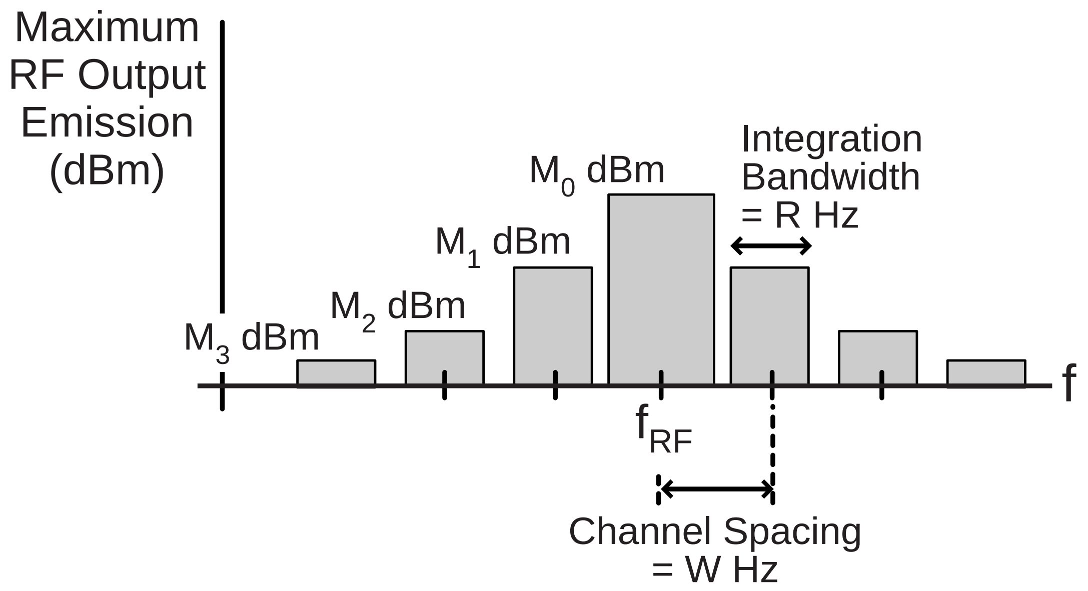
- **Power amplifier**
  - **Nonlinearity will increase out-of-band emission and create harmonic content**
- **Band select filter**
  - **Removes harmonic content, but not out-of-band emission**

Why is Out-of-Band Emission A Problem?



- **Near-far problem**
  - **Interfering transmitter closer to receiver than desired transmitter**
  - **Out-of-emission requirements must be stringent to prevent complete corruption of desired signal**

Specification of Out-of-Band Emissions



- **Maximum radiated power is specified in desired and adjacent channels**
  - **Desired channel power: maximum is M_0 dBm**
  - **Out-of-band emission: maximum power defined as integration of transmitted spectral density over bandwidth R centered at midpoint of each channel offset**

Example – DECT Cordless Telephone Standard

- **Standard for many cordless phones operating at 1.8 GHz**
- **Transmitter Specifications**
  - **Channel spacing: W = 1.728 MHz**
  - **Maximum output power: M_o = 250 mW (24 dBm)**
  - **Integration bandwidth: R = 1 MHz**
  - **Emission mask requirements**

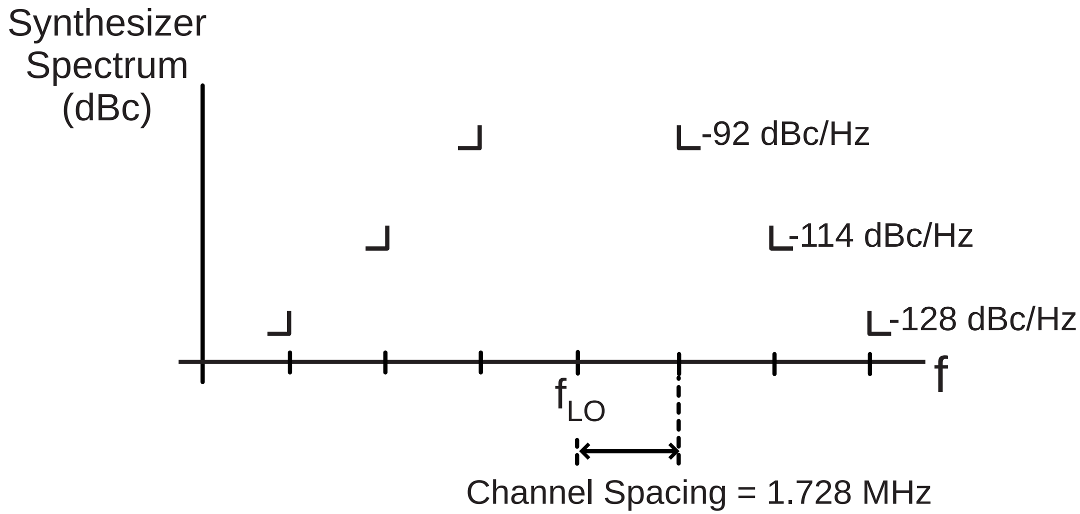
f_{offset} (MHz)	Emission Mask (dBm)
0	M_0 = 24 dBm
1.728	M_1 = -8 dBm
3.456	M_2 = -30 dBm
5.184	M_3 = -44 dBm

Synthesizer Phase Noise Requirements for DECT

- **Calculations (see Lecture 16 of MIT OCW 6.976 for details)**

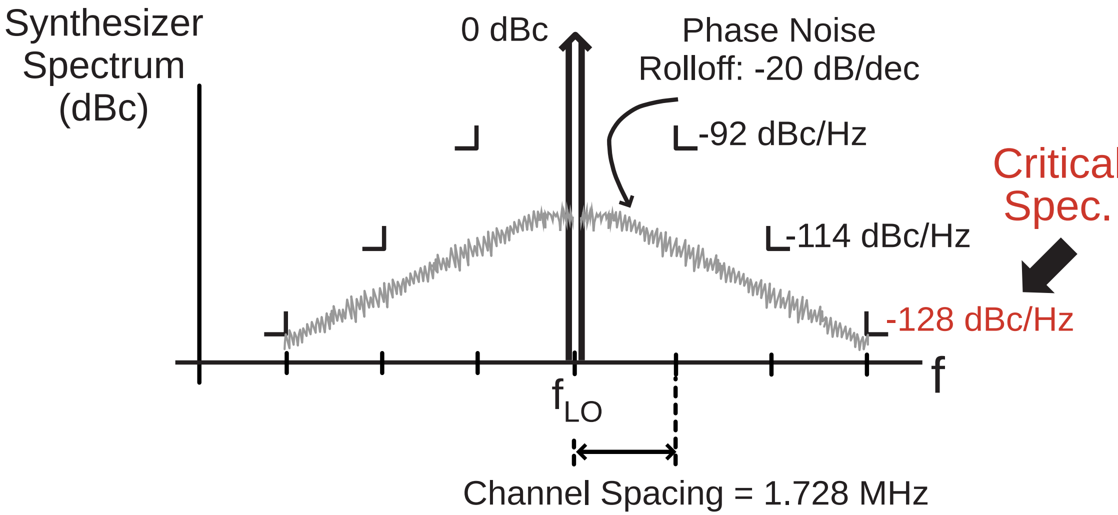
Channel Offset	Mask Power	Maximum Synth. Noise Power in Integration BW	Maximum Synth. Phase Noise at Channel Offset
0	24 dBm	set by required transmit SNR	
1.728 MHz	-8 dBm	X_1 = -29.6 dBc	-92 dBc/Hz
3.456 MHz	-30 dBm	X_2 = -51.6 dBc	-114 dBc/Hz
5.184 MHz	-44 dBm	X_3 = -65.6 dBc	-128 dBc/Hz

- **Graphical display of phase noise mask**

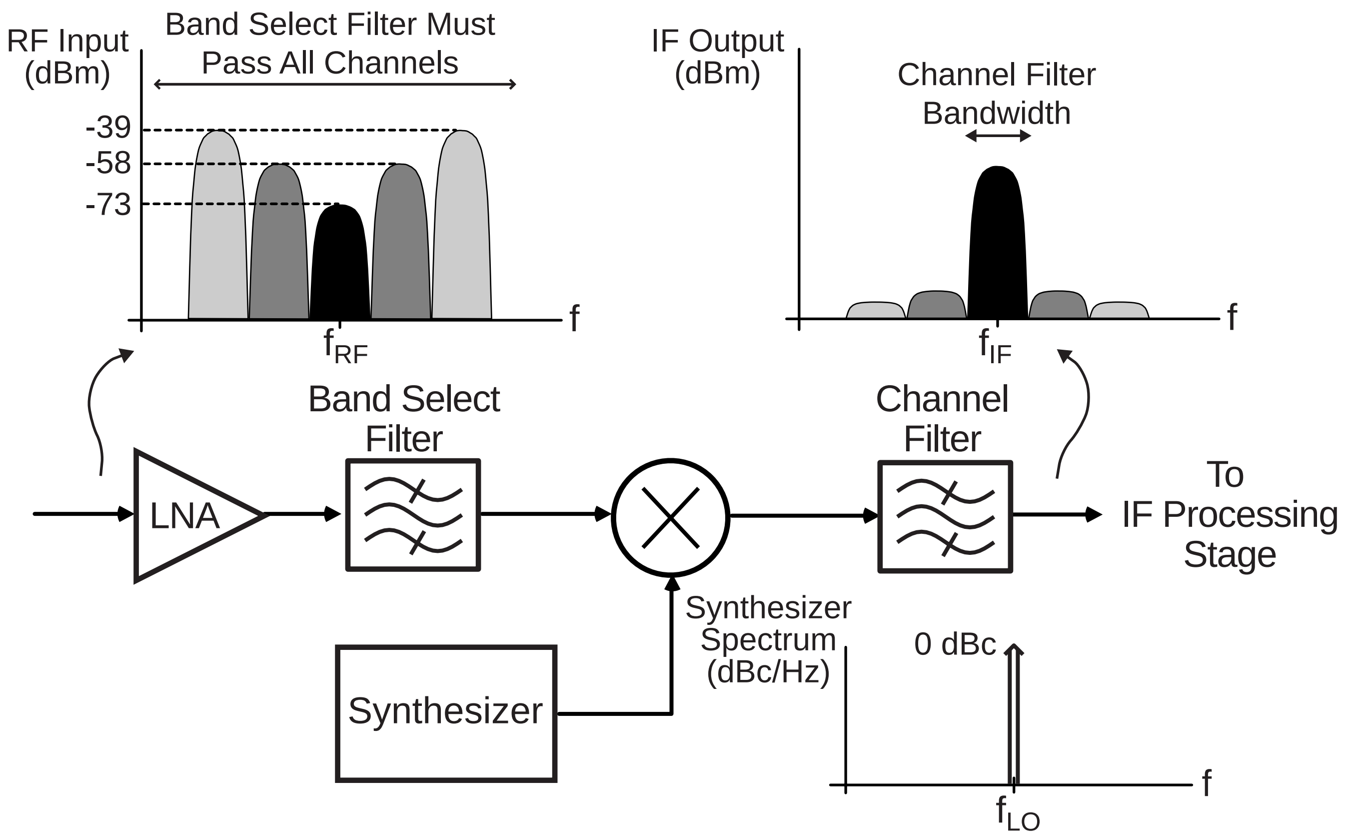


Critical Specification for Phase Noise

- Critical specification is defined to be the one that is hardest to meet with an assumed phase noise rolloff
  - Assume synthesizer phase noise rolls off at -20 dB/decade
    - Corresponds to VCO phase noise characteristic
- For DECT transmitter synthesizer
  - Critical specification is -128 dBc/Hz at 5.184 MHz offset

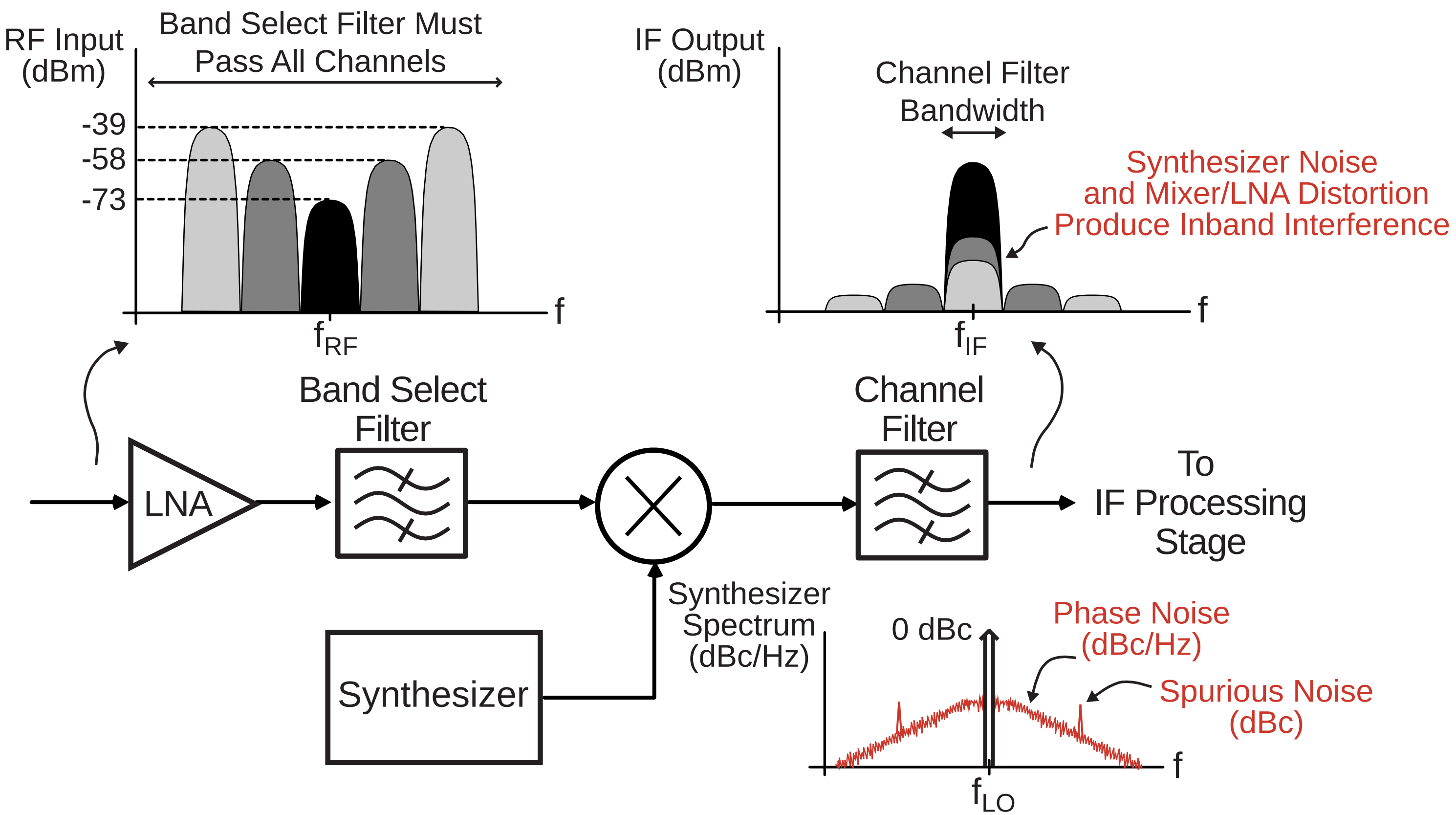


Receiver Blocking Performance



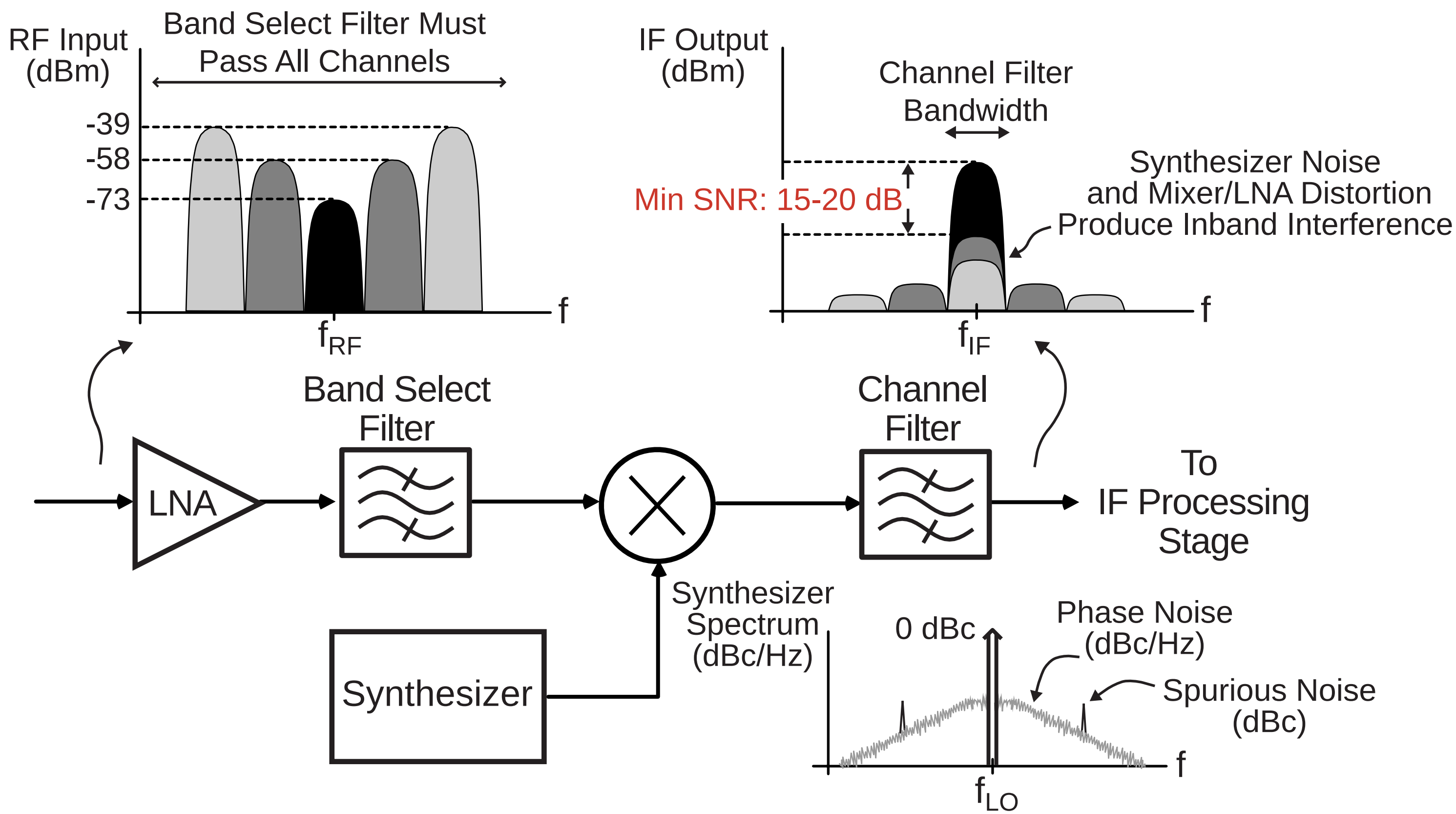
- **Radio receivers must operate in the presence of large interferers (called blockers)**
- **Channel filter plays critical role in removing blockers**
    - Passes desired signal channel, rejects interferers

Impact of Nonidealities on Blocking Performance



- Blockers leak into desired band due to
  - Nonlinearity of LNA and mixer (IIP3)
  - Synthesizer phase and spurious noise
- In-band interference cannot be removed by channel filter!

Quantifying Tolerable In-Band Interference Levels



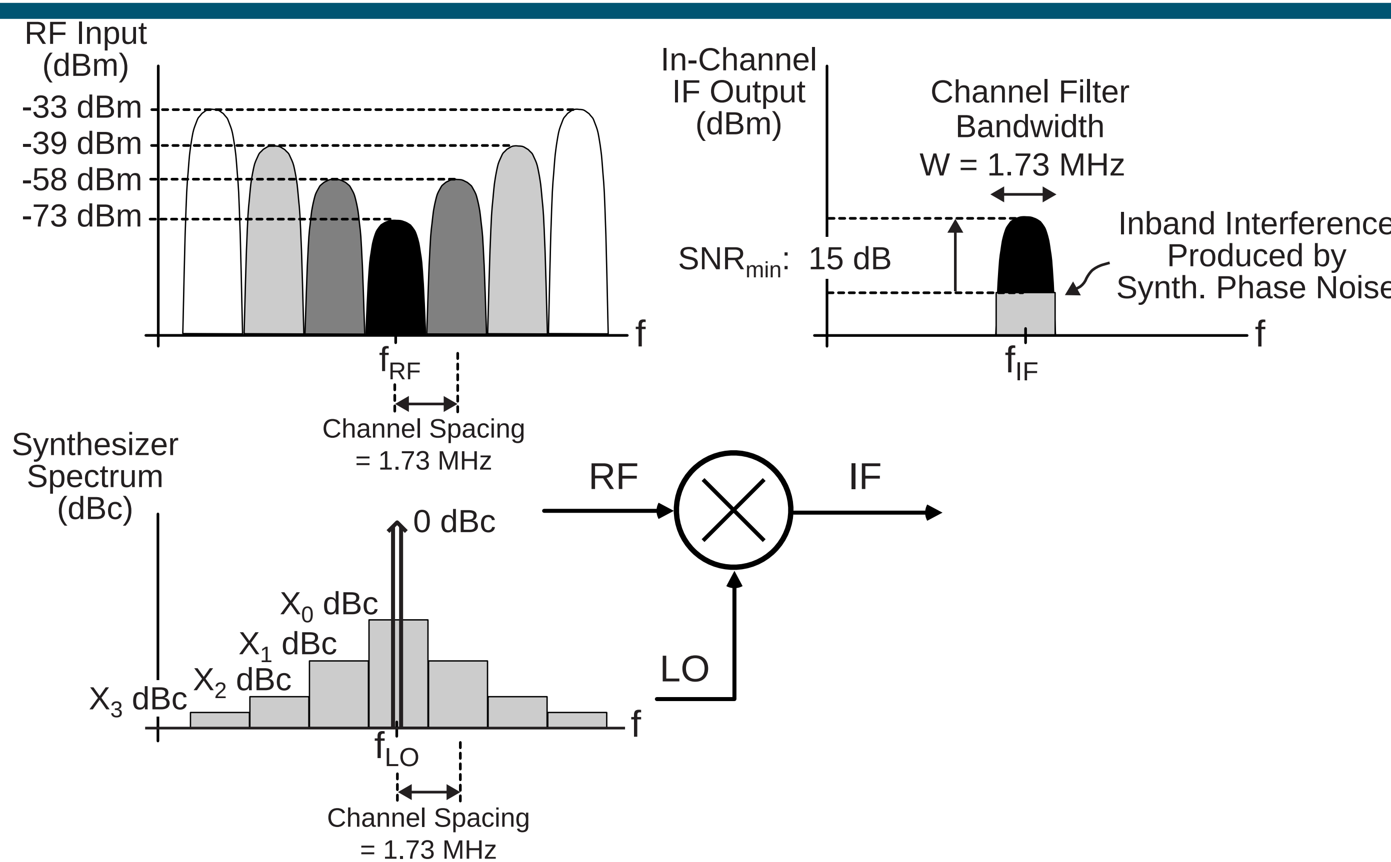
- Digital radios quantify performance with bit error rate (BER)
  - Minimum BER often set at 1e-3 for many radio systems
  - There is a corresponding minimum SNR that must be achieved
- Goal: design so that SNR with interferers is above SNR_{min}

Example – DECT Cordless Telephone Standard

- **Receiver blocking specifications**
  - **Channel spacing: W = 1.728 MHz**
  - **Power of desired signal for blocking test: -73 dBm**
  - **Minimum bit error rate (BER) with blockers: 1e-3**
    - Sets the value of SNR_{min}
      - Perform receiver simulations to determine SNR_{min}
    - Assume SNR_{min} = 15 dB for calculations to follow
  - **Strength of interferers for blocking test**

f_{offset} (MHz)	Blocker Power (dBm)	Relative Strength
1.728	-58 dBm	$Y_1 = 15$ dB
3.456	-39 dBm	$Y_2 = 34$ dB
5.184	-33 dBm	$Y_3 = 40$ dB

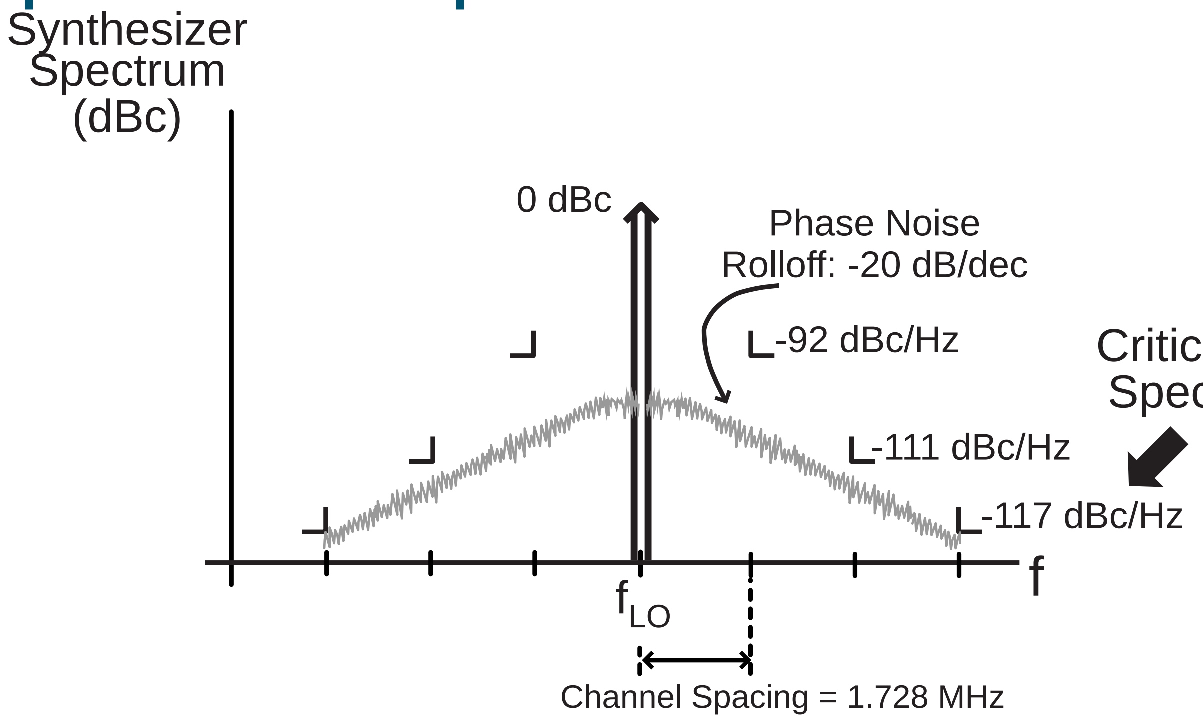
Synthesizer Phase Noise Requirements for DECT



Channel Offset	Relative Blocking Power	Maximum Synth. Noise Power at Channel Offset	Maximum Synth. Phase Noise at Channel Offset
0	0 dB	X_0 = -15 dBc	-77 dBc/Hz
1.728 MHz	Y_1 = 15 dB	X_1 = -30 dBc	-92 dBc/Hz
3.456 MHz	Y_2 = 34 dB	X_2 = -49 dBc	-111 dBc/Hz
5.184 MHz	Y_3 = 40 dB	X_3 = -55 dBc	-117 dBc/Hz

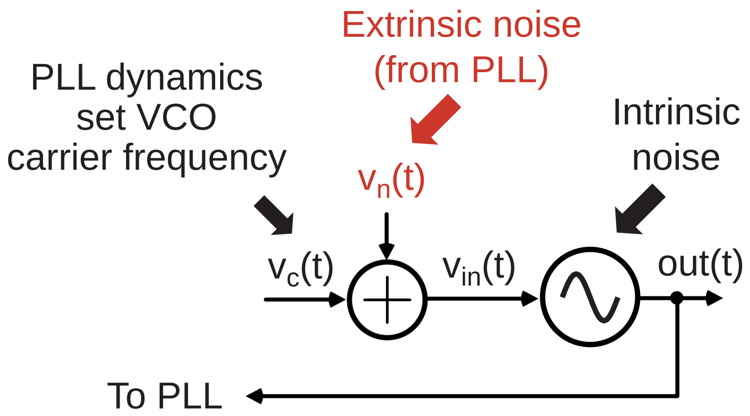
Graphical Display of Required Phase Noise Performance

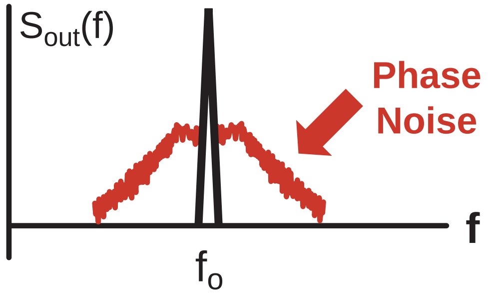
- **Mark phase noise requirements at each offset frequency**



- **Calculate critical specification for receive synthesizer**
  - **Critical specification is -117 dBc/Hz at 5.184 MHz offset**
    - Lower performance demanded of receiver synthesizer than transmitter synthesizer in DECT applications!

Noise Modeling for Frequency Synthesizers

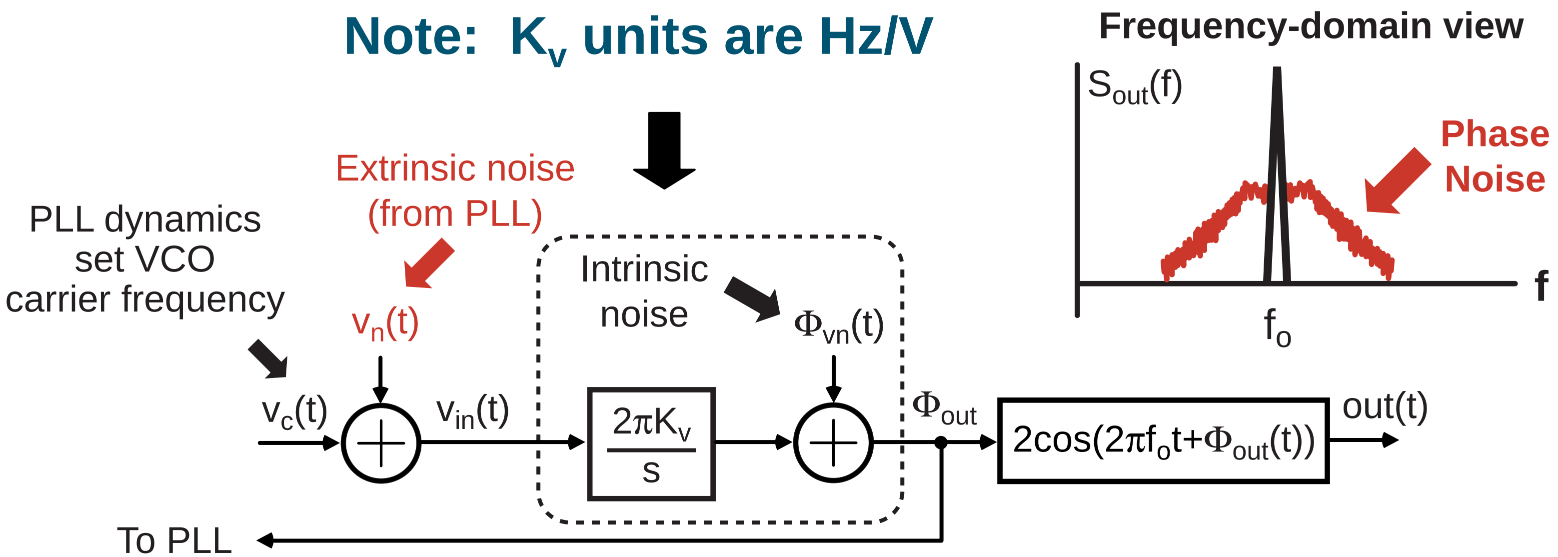




- **PLL has an impact on VCO noise in two ways**
  - **Adds noise from various PLL circuits**
  - **Suppresses low frequency VCO noise through PLL feedback**
- **Focus on modeling the above based on phase deviations**
  - **Simpler than dealing directly with PLL sine wave output**

Phase Deviation Model for Noise Analysis

Note: K_v units are Hz/V



- **Model the impact of noise on instantaneous phase**
  - **Relationship between PLL output and instantaneous phase**

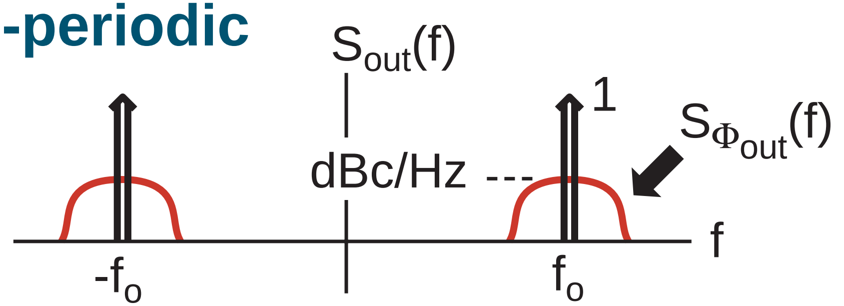
$$out(t) = 2\cos(2\pi f_o t + \underline{\Phi_{out}(t)})$$

  - **Output spectrum**

$$S_{out}(f) = S_{sin}(f) + S_{sin}(f) * S_{\Phi_{out}}$$

Phase Noise Versus Spurious Noise

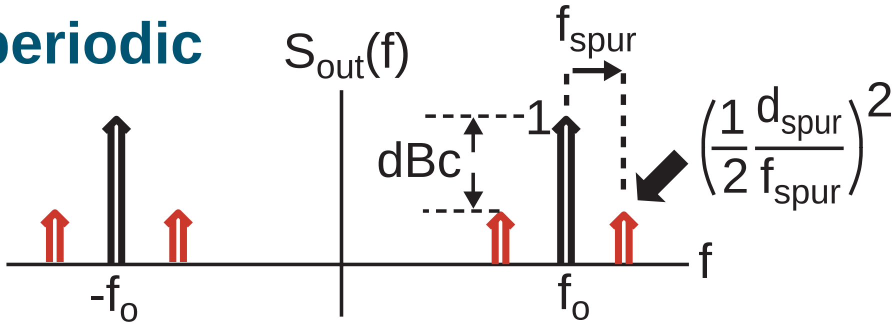
- **Phase noise is non-periodic**



  - **Described as a spectral density relative to carrier power**

$$L(f) = 10\log(S_{\Phi_{out}}(f))\ \mathrm{dBc/Hz}$$

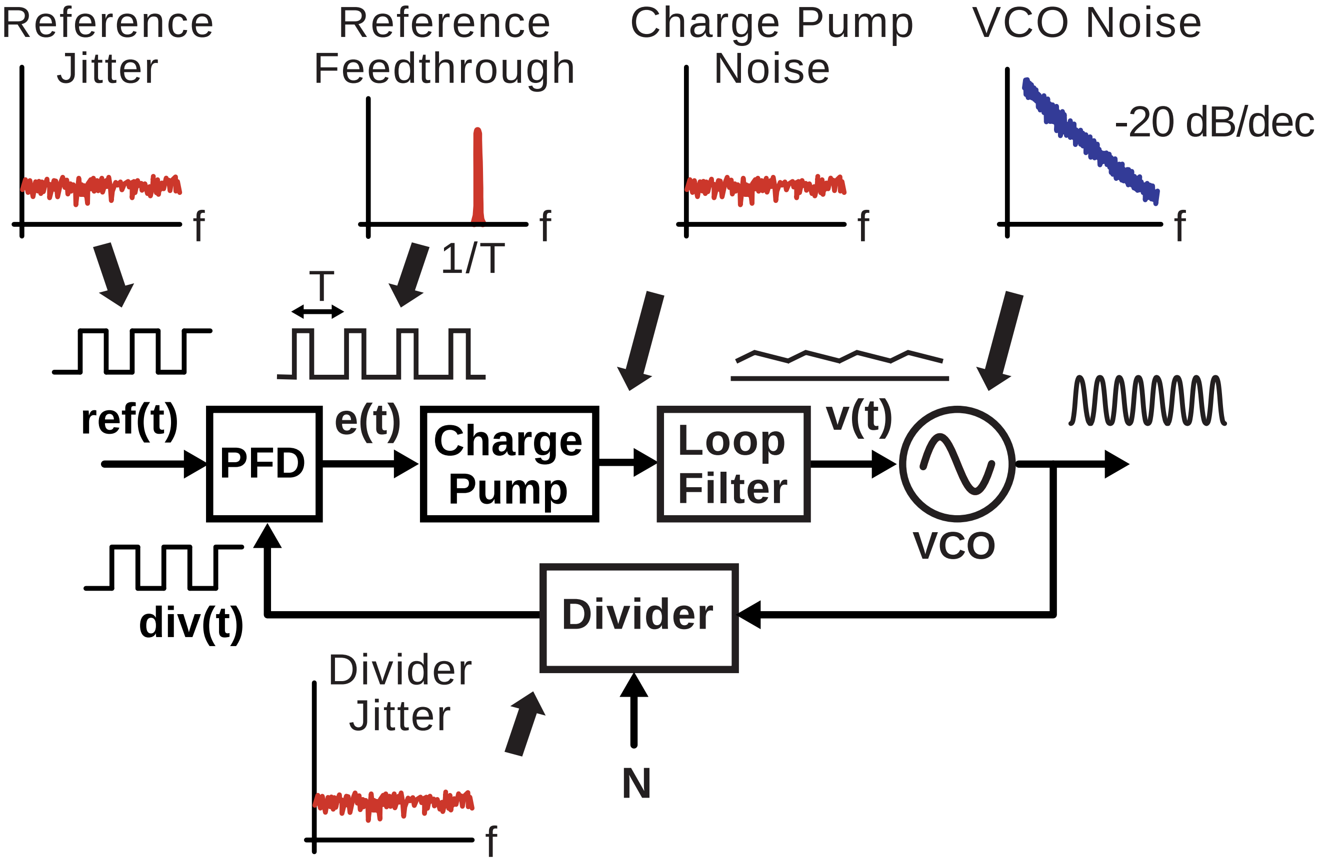
- **Spurious noise is periodic**



  - **Described as tone power relative to carrier power**

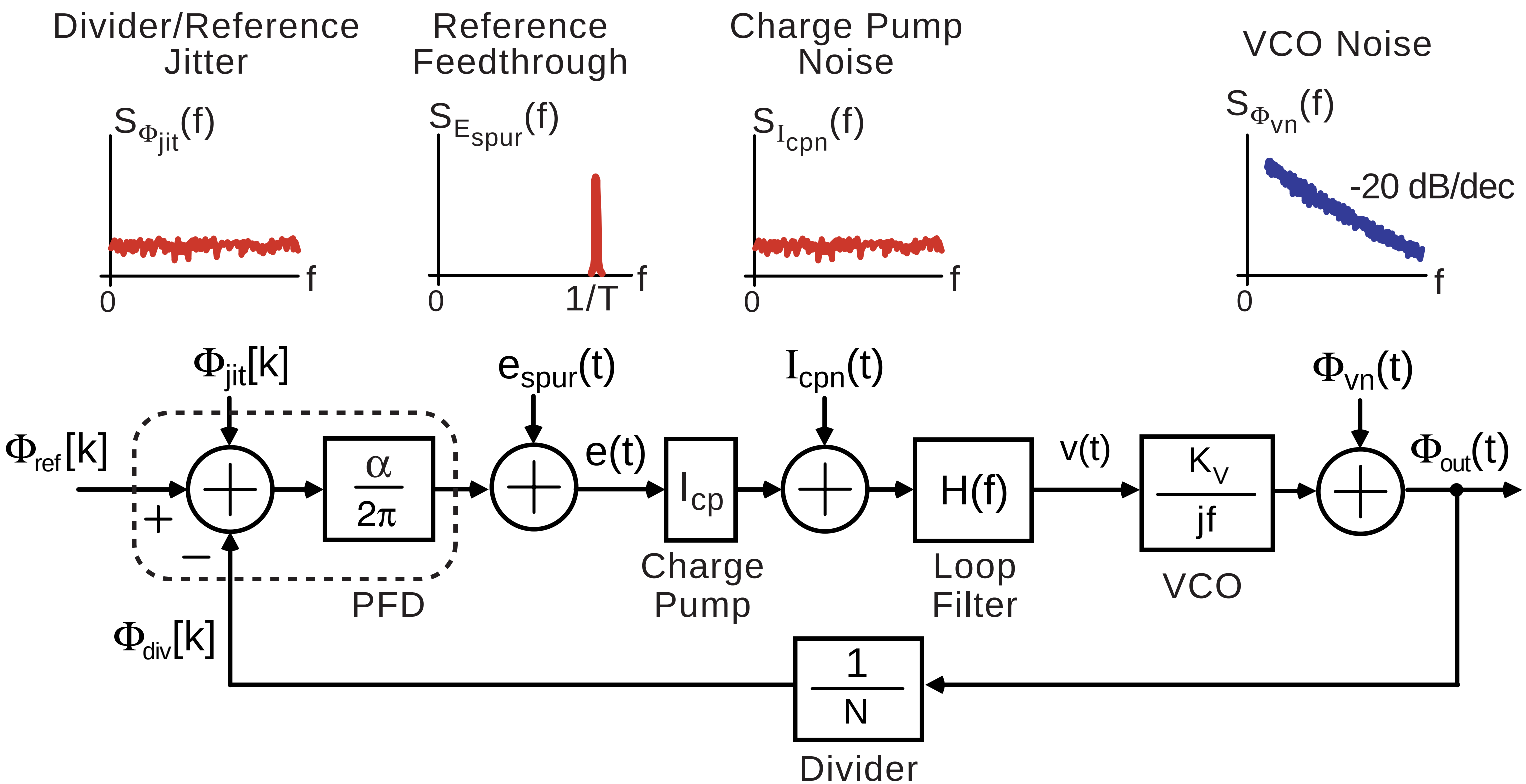
$$20\log\left(\frac{d_{spur}}{2f_{spur}}\right)\ \mathrm{dBc}$$

Sources of Noise in Frequency Synthesizers



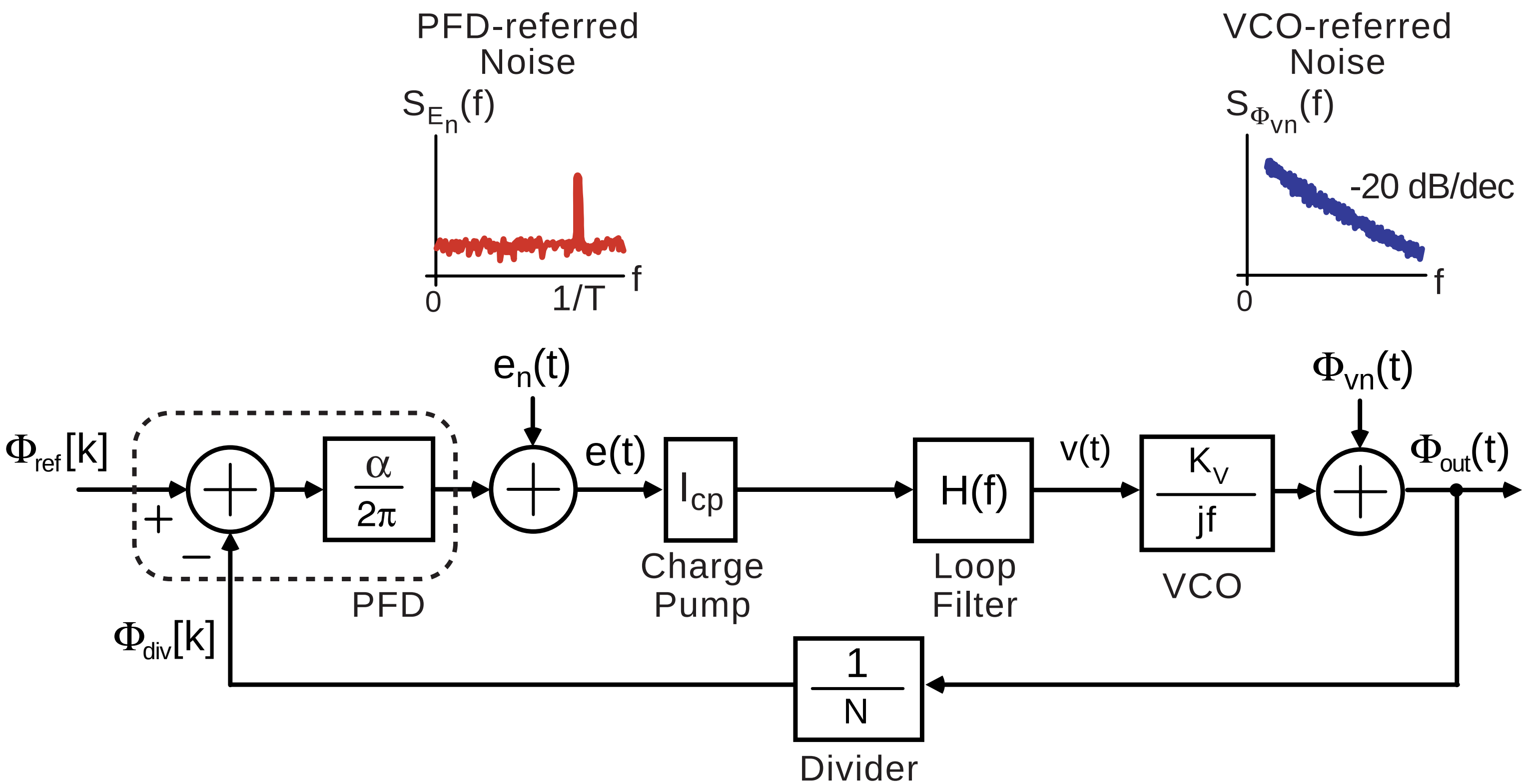
- **Extrinsic noise sources to VCO**
  - **Reference/divider jitter and reference feedthrough**
  - **Charge pump noise**

Modeling the Impact of Noise on Output Phase of PLL



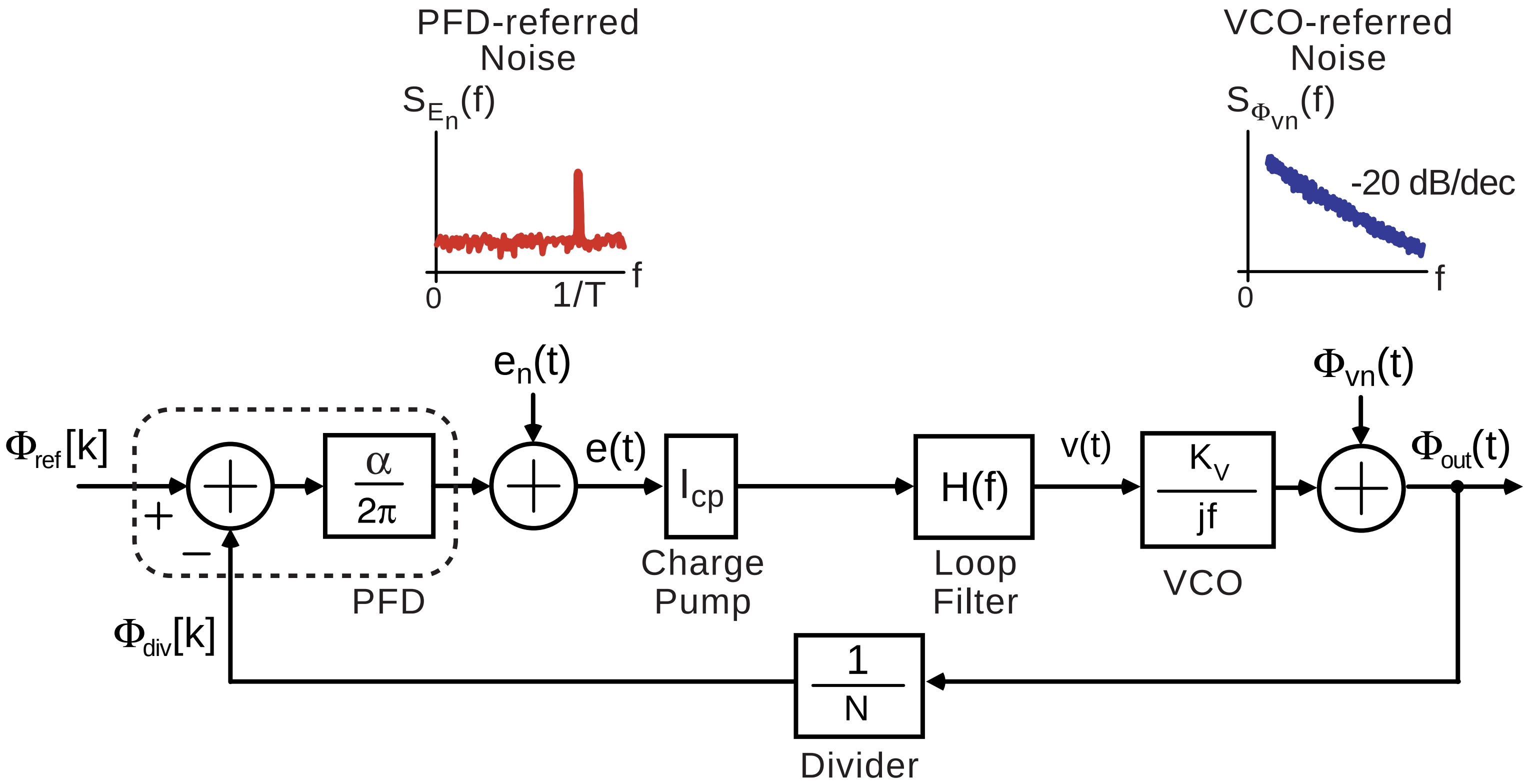
- **Determine impact on output phase by deriving transfer function from each noise source to PLL output phase**
  - **There are a lot of transfer functions to keep track of!**

Simplified Noise Model



- **Refer all PLL noise sources (other than the VCO) to the PFD output**
  - **PFD-referred noise corresponds to the sum of these noise sources referred to the PFD output**

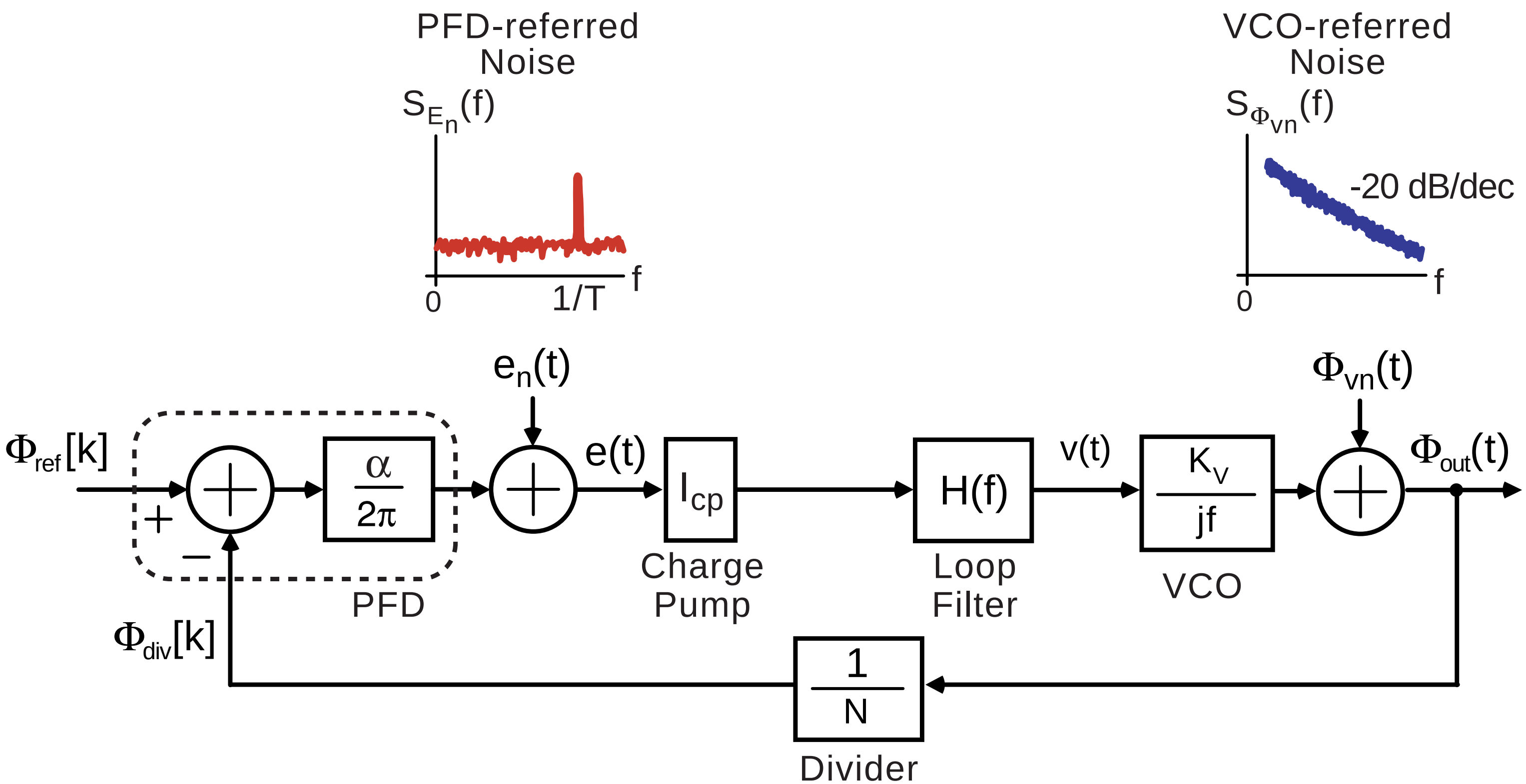
Impact of PFD-referred Noise on Synthesizer Output



- **Transfer function derived using Black's formula**

$$\frac{\Phi_{out}}{e_n} = \frac{I_{cp}H(f)K_v/(jf)}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

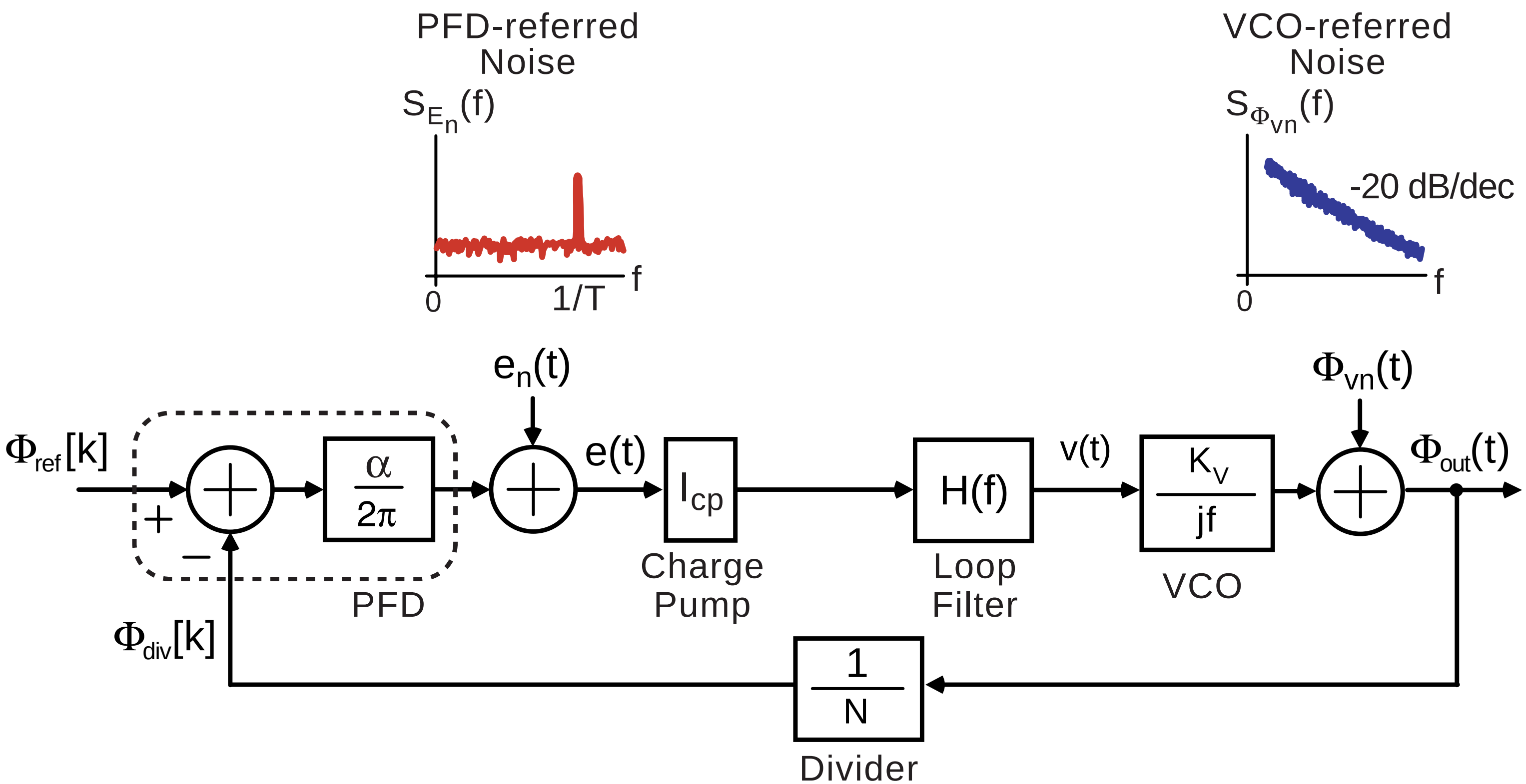
Impact of VCO-referred Noise on Synthesizer Output



- **Transfer function again derived from Black's formula**

$$\frac{\Phi_{out}}{e_n} = \frac{1}{1 + \alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

A Simpler Parameterization for PLL Transfer Functions



- **Define G(f) as**

$$G(f) = \frac{A(f)}{1 + A(f)}$$

Always has a gain of one at DC

  - **A(f) is the open loop transfer function of the PLL**

$$A(f) = \alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)$$

Parameterize Noise Transfer Functions in Terms of G(f)

- **PFD-referred noise**

$$\frac{\Phi_{out}}{e_n} = \frac{I_{cp}H(f)K_v/(jf)}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

$$= \frac{2\pi}{\alpha}N\frac{\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

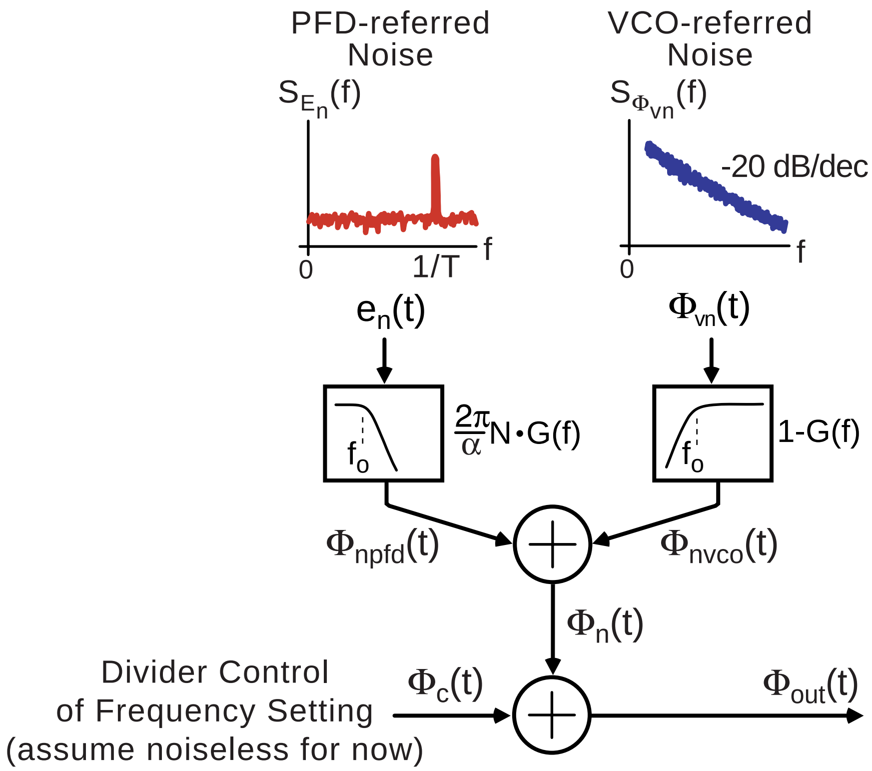
$$= \frac{2\pi}{\alpha}N\frac{A(f)}{1+A(f)} = \boxed{\frac{2\pi}{\alpha}NG(f)}$$

- **VCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_{vn}} = \frac{1}{1+\alpha/(2\pi)I_{cp}H(f)K_v/(jf)(1/N)}$$

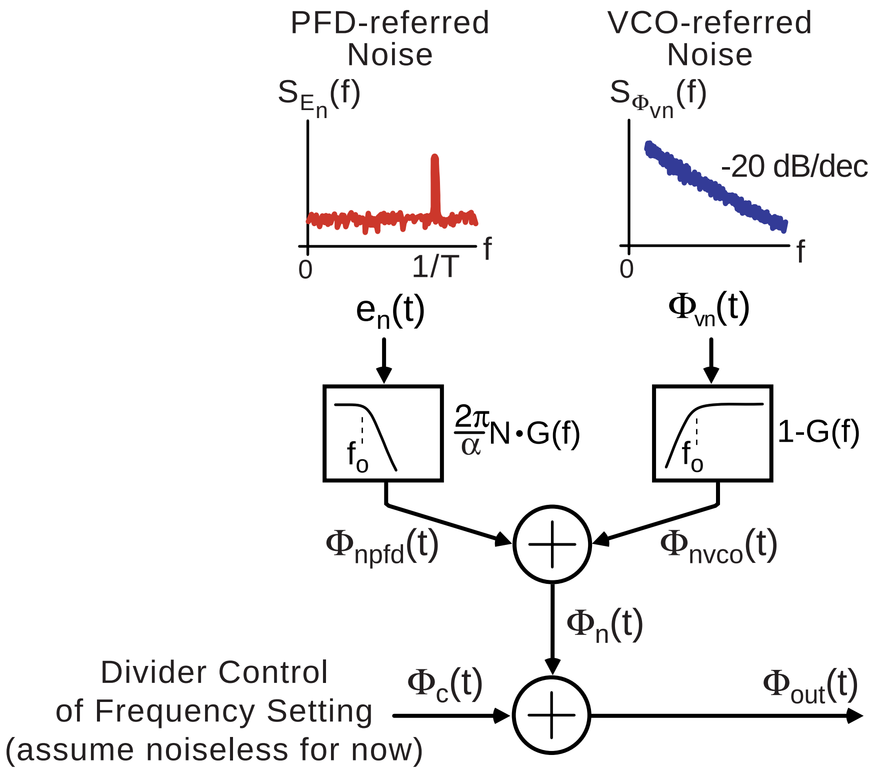
$$= \frac{1}{1+A(f)} = 1 - \frac{A(f)}{1+A(f)} = \boxed{1-G(f)}$$

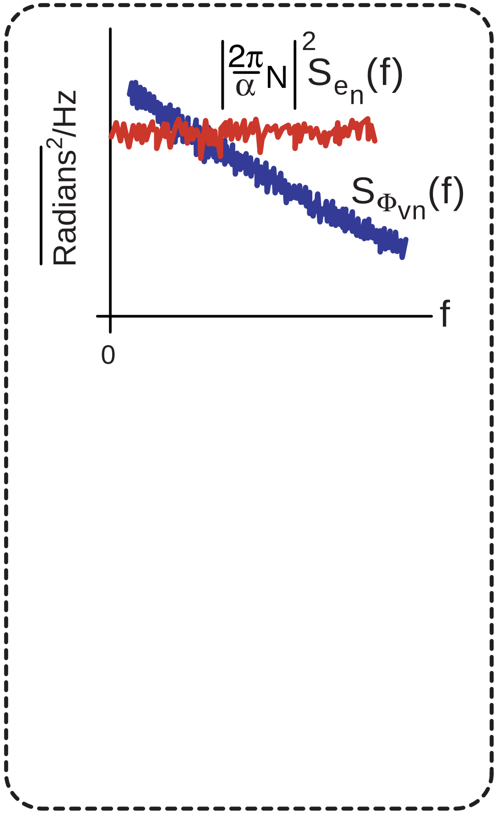
Parameterized PLL Noise Model



- PFD-referred noise is lowpass filtered
- VCO-referred noise is highpass filtered
- Both filters have the same transition frequency values
  - Defined as f_o

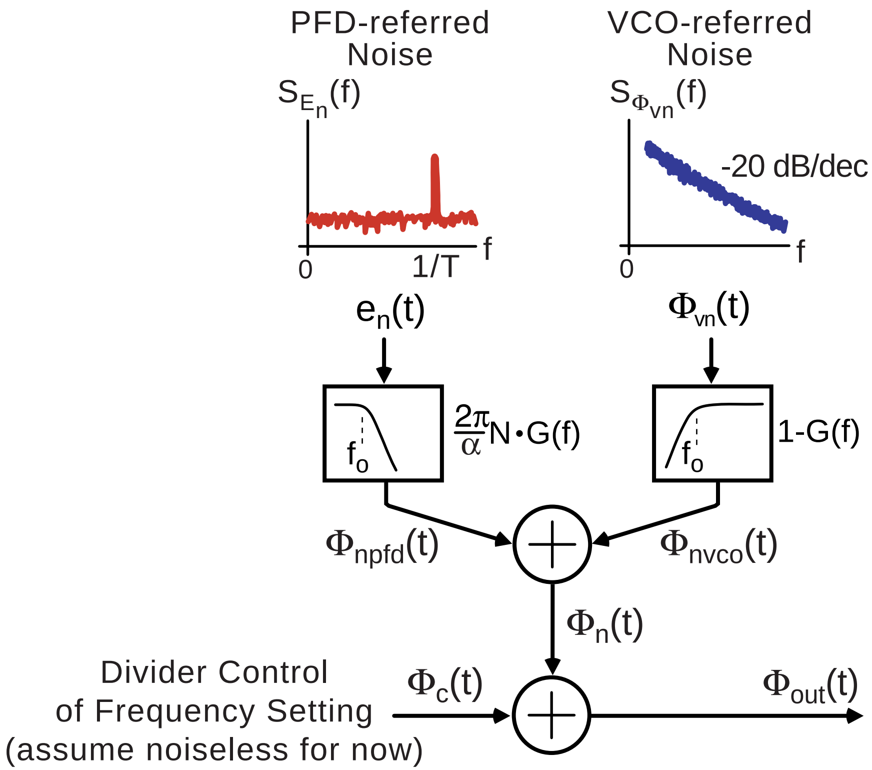
Impact of PLL Parameters on Noise Scaling

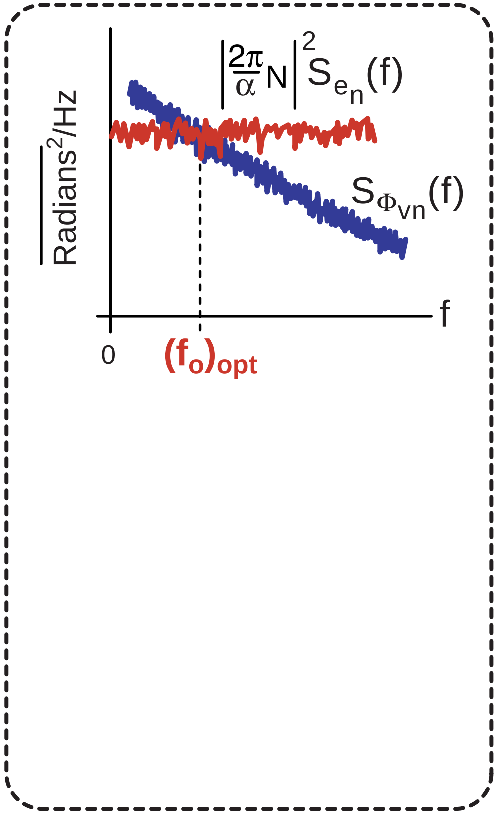




- **PFD-referred noise is scaled by square of divide value and inverse of PFD gain**
  - **High divide values lead to large multiplication of this noise**
- **VCO-referred noise is not scaled (only filtered)**

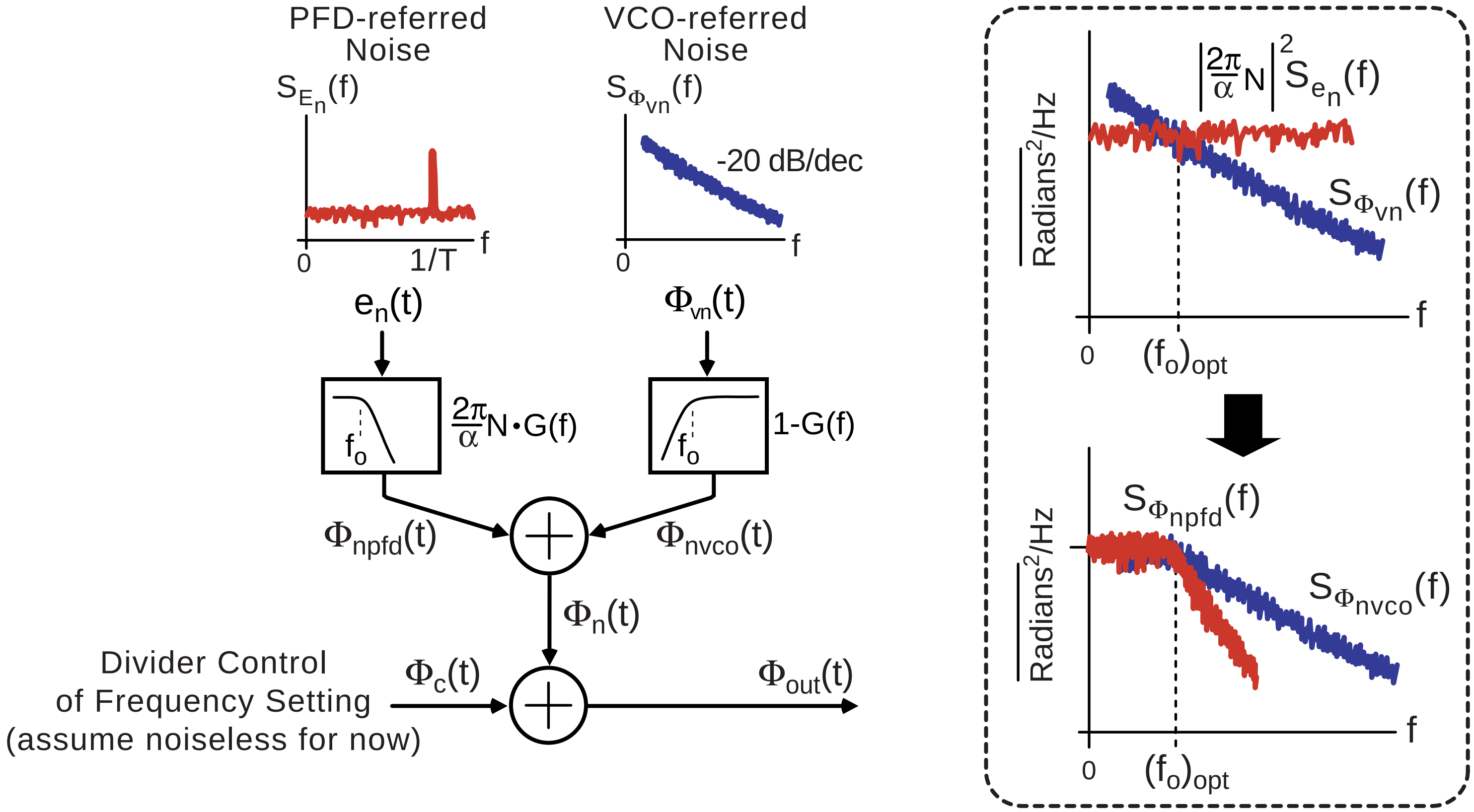
Optimal Bandwidth Setting for Minimum Noise





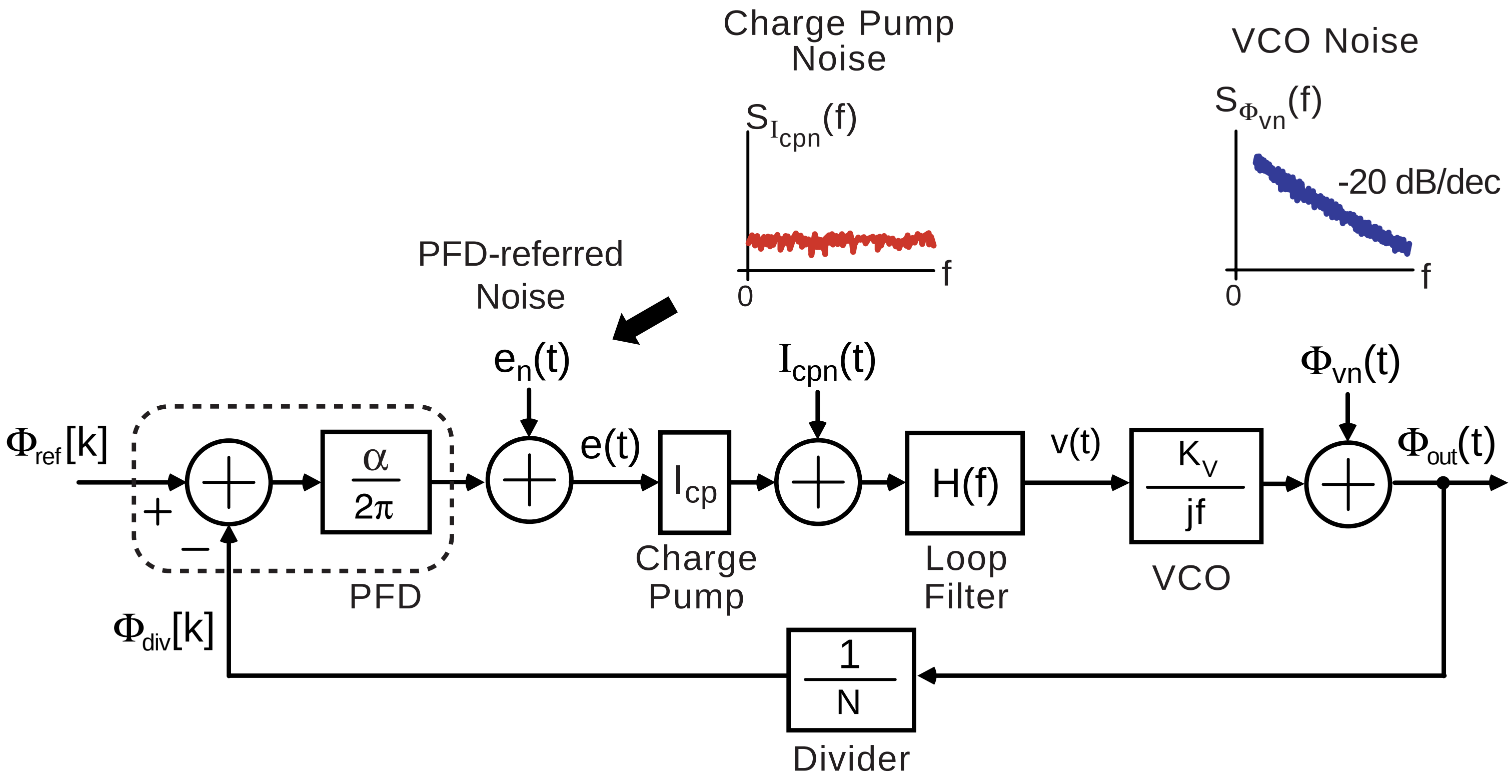
- **Optimal bandwidth is where scaled noise sources meet**
  - **Higher bandwidth will pass more PFD-referred noise**
  - **Lower bandwidth will pass more VCO-referred noise**

Resulting Output Noise with Optimal Bandwidth



- **PFD-referred noise dominates at low frequencies**
  - **Corresponds to close-in phase noise of synthesizer**
- **VCO-referred noise dominates at high frequencies**
  - **Corresponds to far-away phase noise of synthesizer**

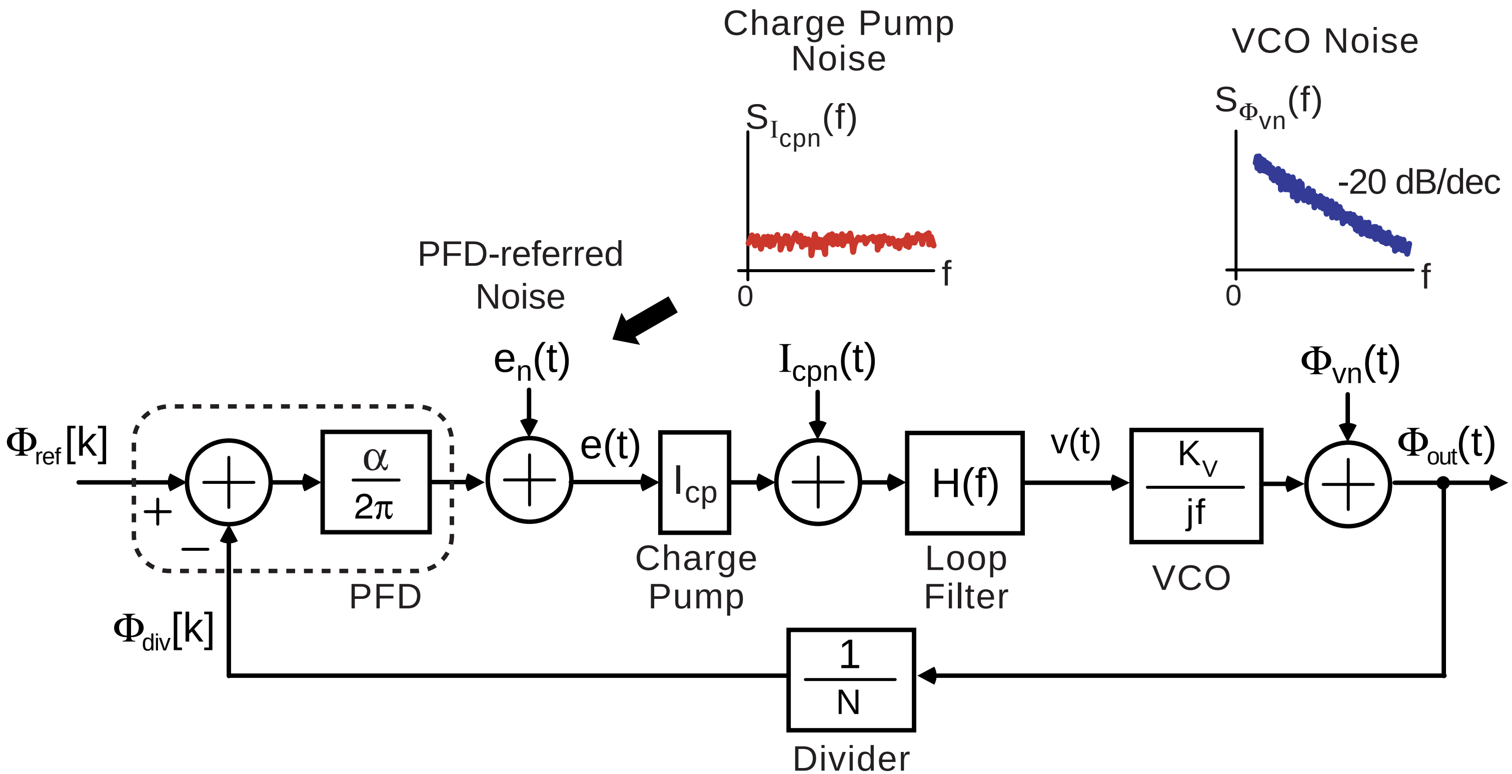
Analysis of Charge Pump Noise Impact



- **We can refer charge pump noise to PFD output by simply scaling it by $1/I_{cp}$**

$$\frac{\Phi_{out}}{I_{cpn}} = \left(\frac{1}{I_{cp}}\right)\frac{\Phi_{out}}{e_n} = \left(\frac{1}{I_{cp}}\right)\frac{2\pi}{\alpha}NG(f)$$

Calculation of Charge Pump Noise Impact

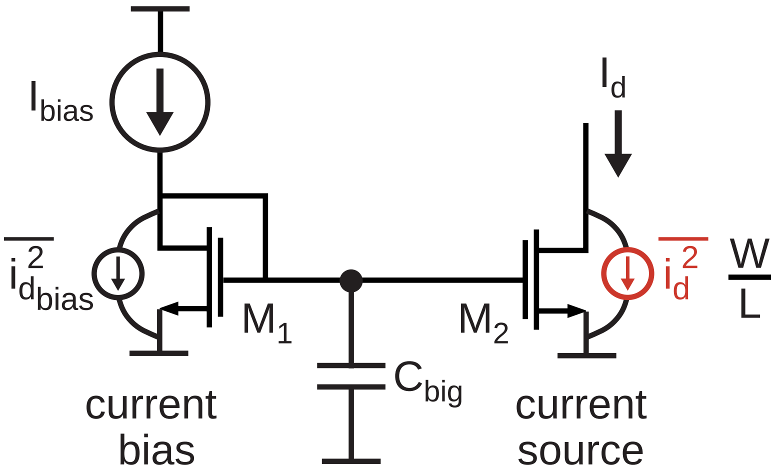


- **Contribution of charge pump noise to overall output noise**

$$S_{\Phi_{out}}(f) = \left(\frac{1}{I_{cp}}\right)^2 \left(\frac{2\pi}{\alpha}N\right)^2 |G(f)|^2 S_{I_{cpn}}(f) + \text{other sources}$$

  - **Need to determine impact of I_{cp} on $S_{Icpn}(f)$**

Impact of Transistor Current Value on its Noise



- **Charge pump noise will be related to the current it creates as**

$$S_{I_{cpn}}(f) \propto \frac{\overline{I_d^2}}{\Delta f} = 4kT\gamma g_{do}$$

- **Recall that g_{do} is the channel resistance at zero V_{ds}**
  - **At *a fixed current density*, we have**

$$g_{do} \propto W \propto I_d \Rightarrow \boxed{\overline{I_d^2} \propto I_d}$$

Impact of Charge Pump Current Value on Output Noise

- **Recall**

$$S_{\Phi_{out}}(f) = \left(\frac{1}{I_{cp}}\right)^2 \left(\frac{2\pi}{\alpha}N\right)^2 |G(f)|^2 S_{I_{cpn}}(f) + \text{other sources}$$

- **Given previous slide, we can say**

$$S_{I_{cpn}}(f) \propto I_{cp}$$

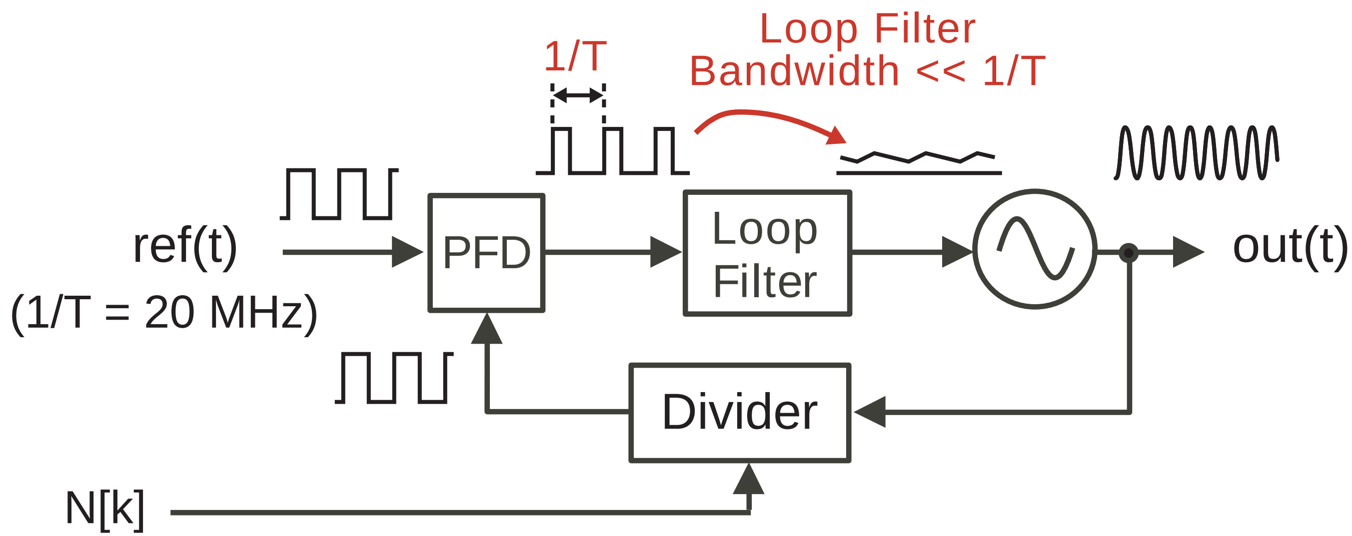
  - **Assumes a fixed current density for the key transistors in the charge pump as I_{cp} is varied**
- **Therefore**

$$S_{\Phi_{out}}(f) \Big|_{\text{charge pump}} \propto \frac{1}{I_{cp}}$$

  - **Want high charge pump current to achieve low noise**
  - **Limitation set by power and area considerations**

Fractional-N Frequency Synthesizers

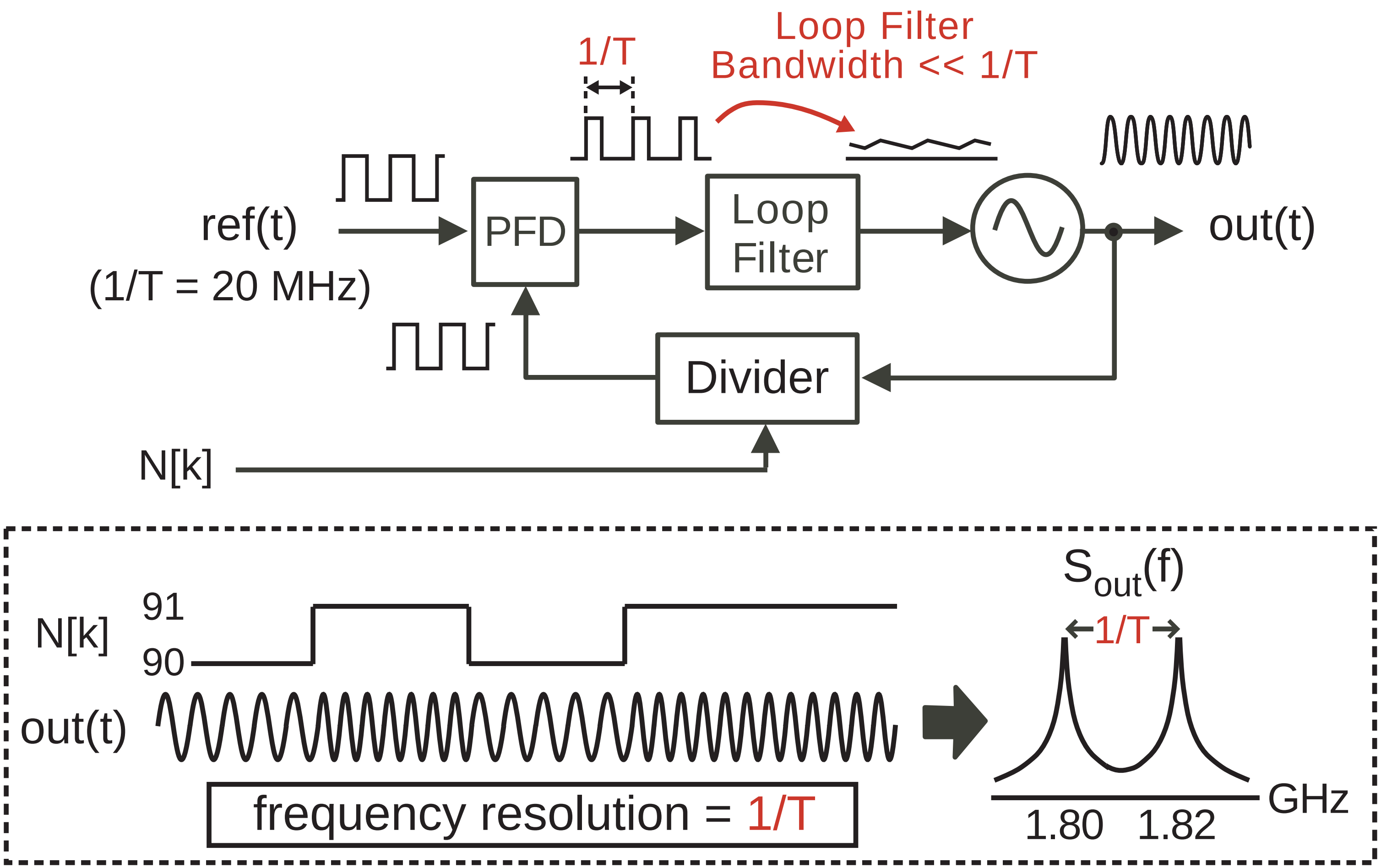
Bandwidth Constraints for Integer-N Synthesizers



- **PFD output has a periodicity of 1/T**
  - **1/T = reference frequency**
- **Loop filter must have a bandwidth << 1/T**
  - **PFD output pulses must be filtered out and average value extracted**

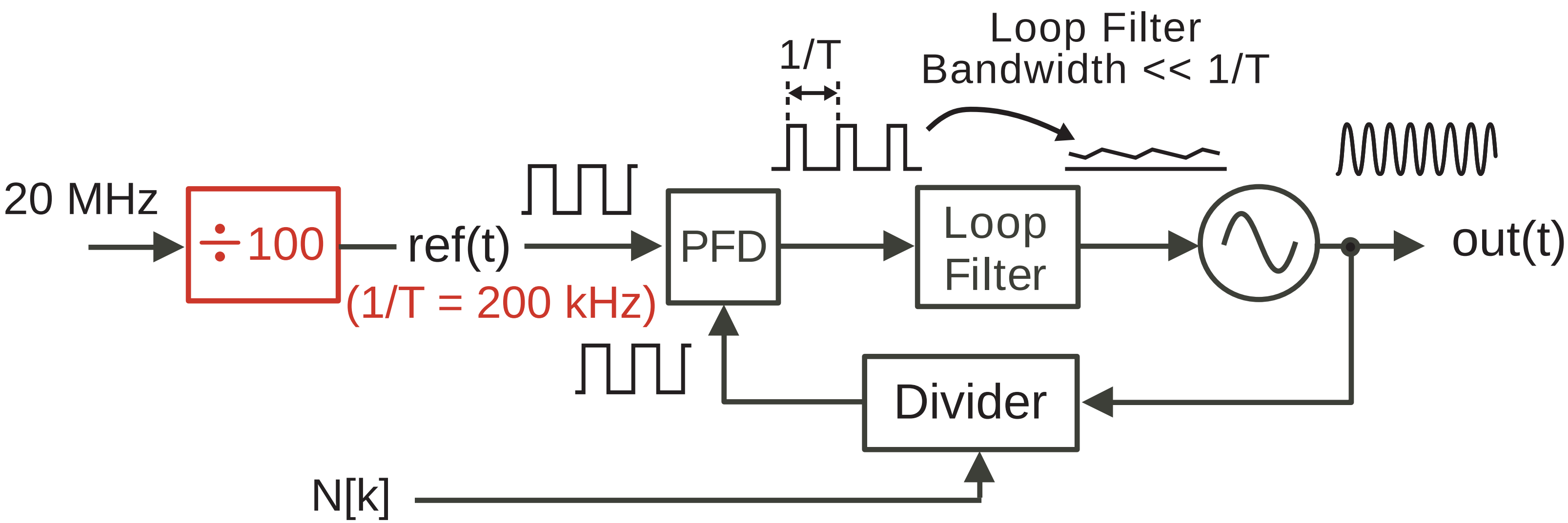
Closed loop PLL bandwidth often chosen to be a factor of ten lower than 1/T

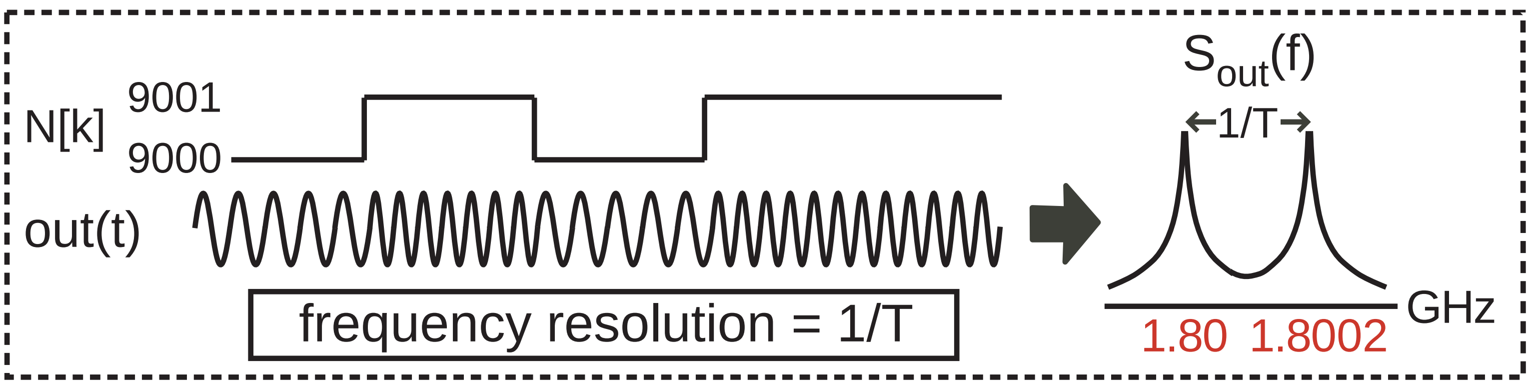
Bandwidth Versus Frequency Resolution



- Frequency resolution set by reference frequency (1/T)
  - Higher resolution achieved by lowering 1/T

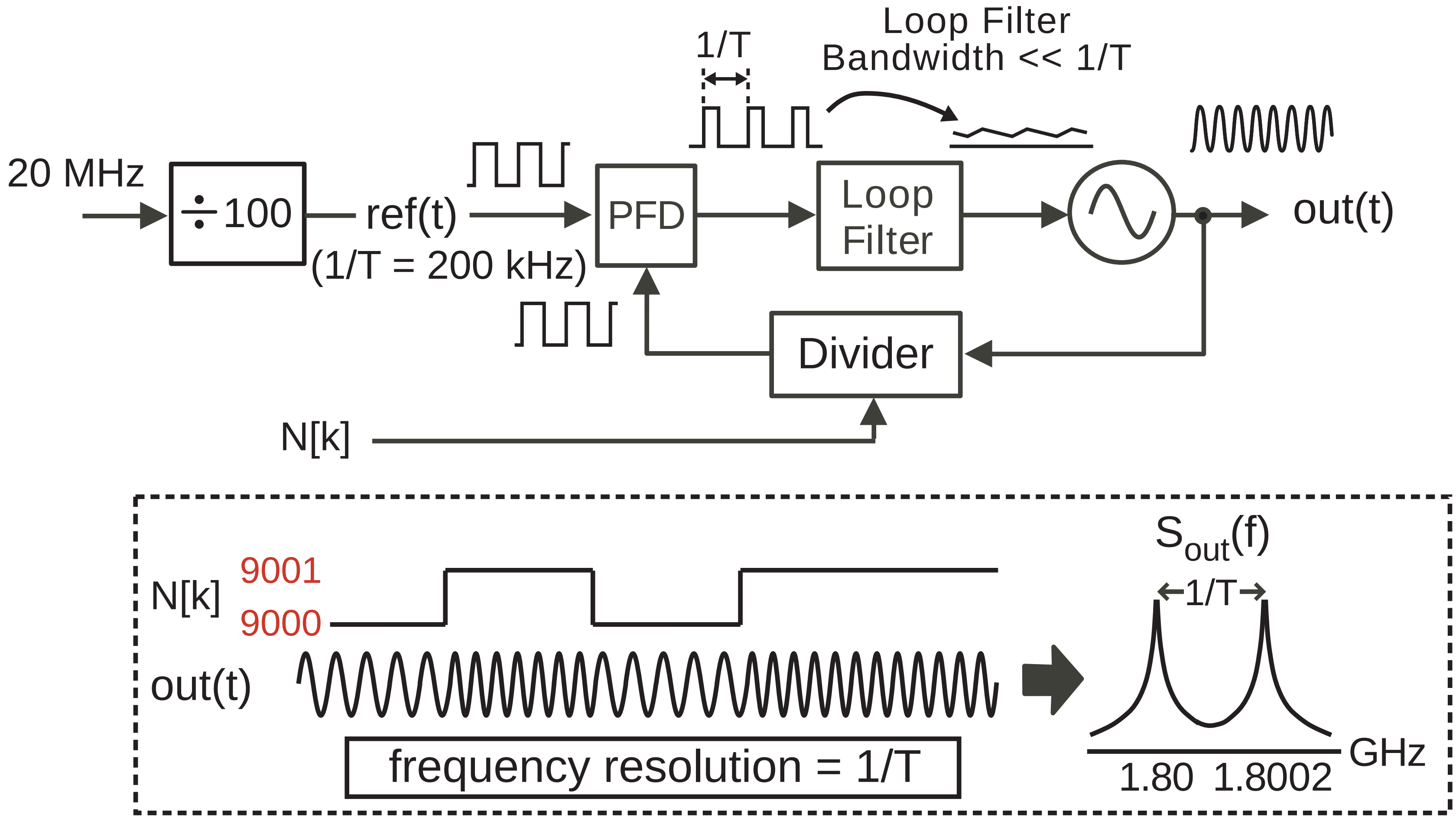
Increasing Resolution in Integer-N Synthesizers





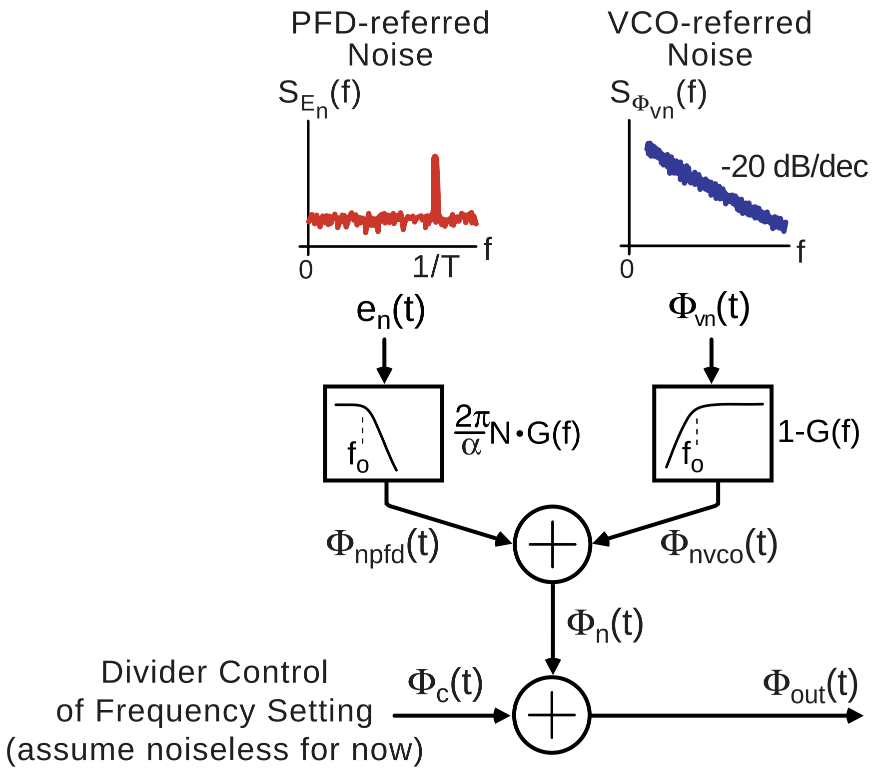
- **Use a reference divider to achieve lower 1/T**
  - **Leads to a low PLL bandwidth (< 20 kHz here)**

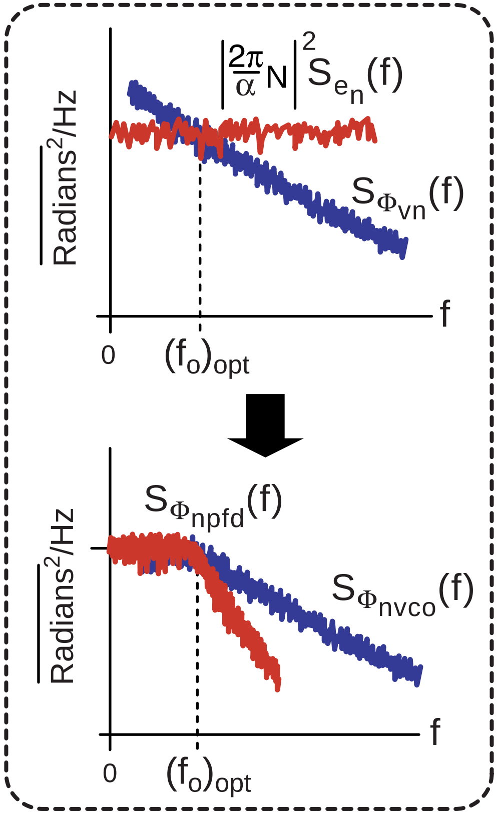
The Issue of Noise



- **Lower 1/T leads to higher divide value**
  - **Increases PFD noise at synthesizer output**

Modeling PFD Noise Multiplication

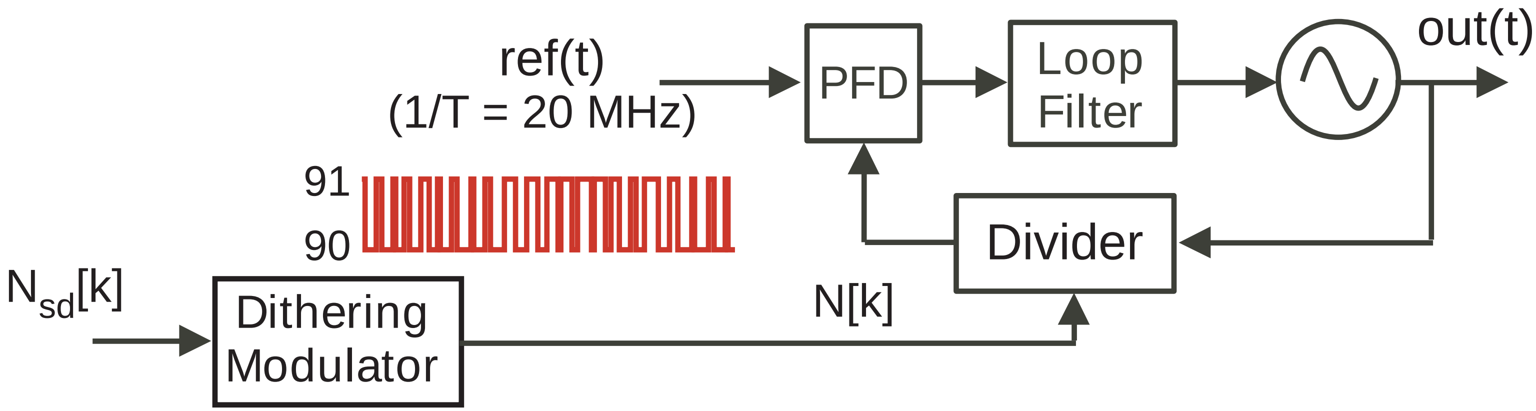


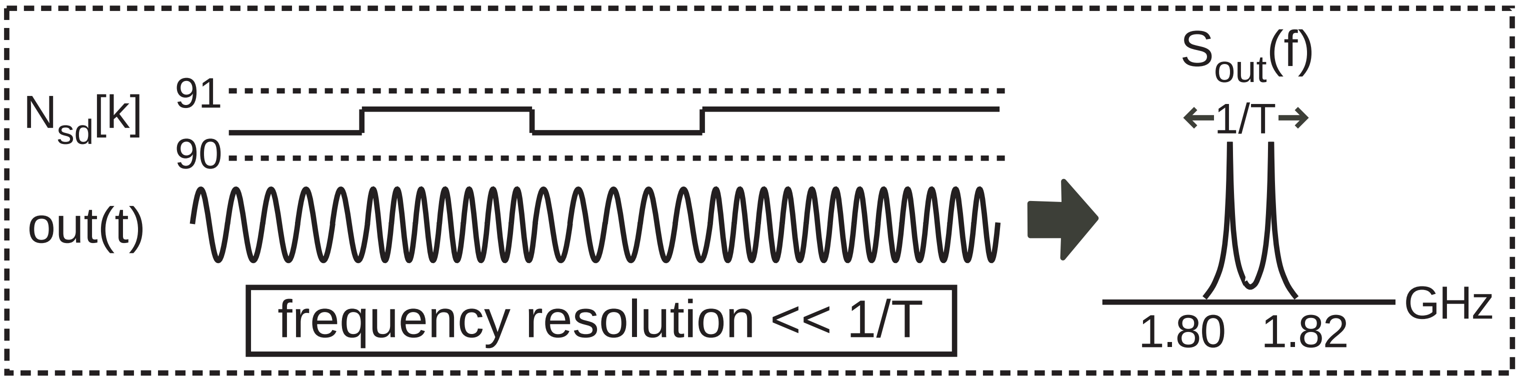


- **Influence of PFD noise seen in above model**
  - **PFD spectral density multiplied by N^2 before influencing PLL output phase noise**

High divide values ➡ high phase noise at low frequencies

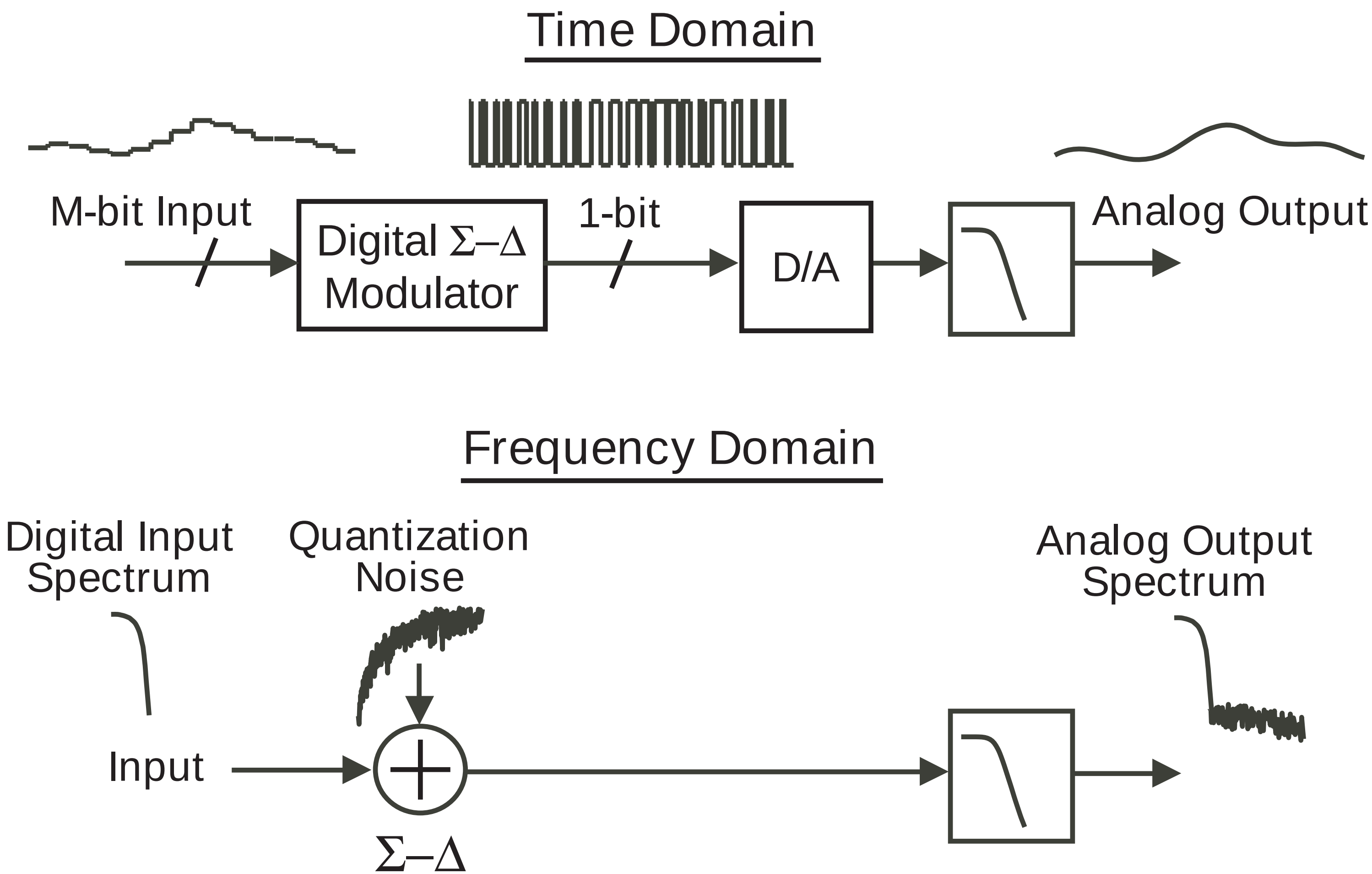
Fractional-N Frequency Synthesizers





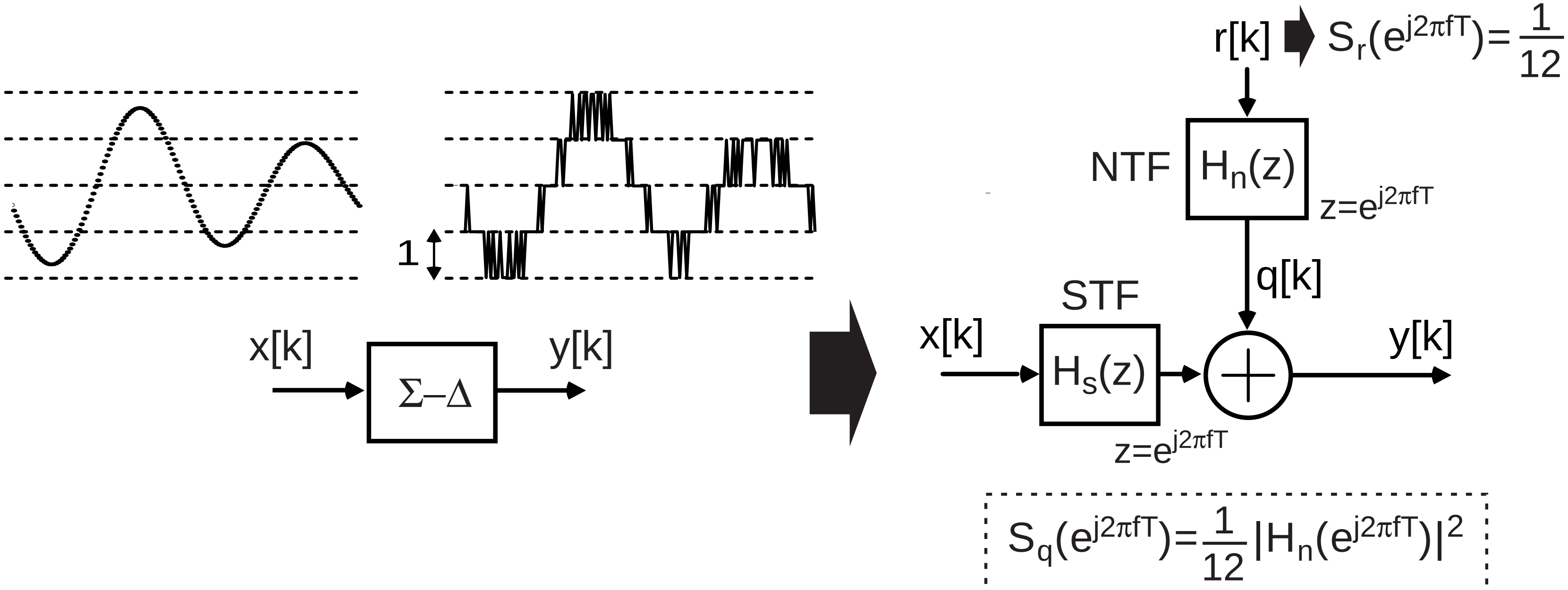
- **Break constraint that divide value be integer**
  - **Dither divide value dynamically to achieve fractional values**
  - **Frequency resolution is now arbitrary regardless of 1/T**
- **Want high 1/T to allow a high PLL bandwidth**

A Nice Dithering Method: Sigma-Delta Modulation



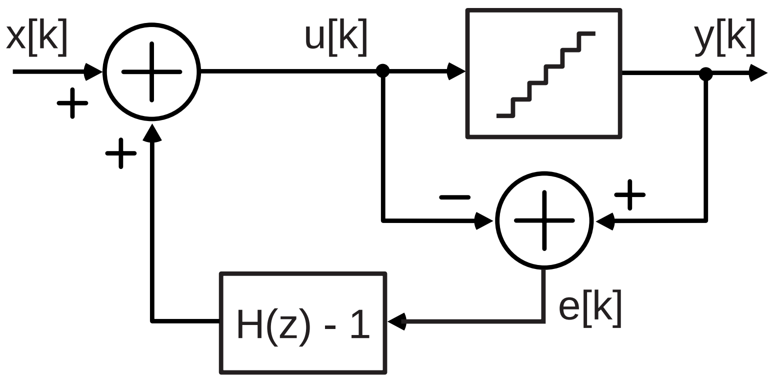
- **Sigma-Delta dithers in a manner such that resulting quantization noise is "shaped" to high frequencies**

Linearized Model of Sigma-Delta Modulator



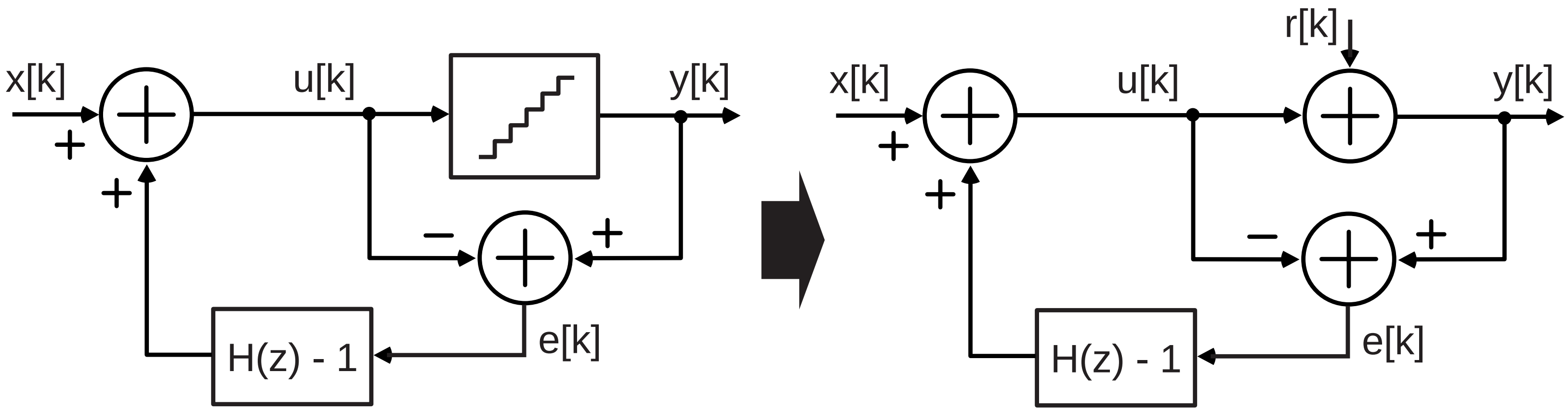
- **Composed of two transfer functions relating input and noise to output**
  - **Signal transfer function (STF)**
    - Filters input (generally undesirable)
  - **Noise transfer function (NTF)**
    - Filters (i.e., shapes) noise that is assumed to be white

Example: Cutler Sigma-Delta Topology



- **Output is quantized in a multi-level fashion**
- **Error signal, e[k], represents the quantization error**
- **Filtered version of quantization error is fed back to input**
  - **H(z) is typically a highpass filter whose first tap value is 1**
    - i.e., $H(z) = 1 + a_1 z^{-1} + a_2 z^{-2} \cdots$
  - **H(z) – 1 therefore has a first tap value of 0**
    - Feedback needs to have delay to be realizable

Linearized Model of Cutler Topology

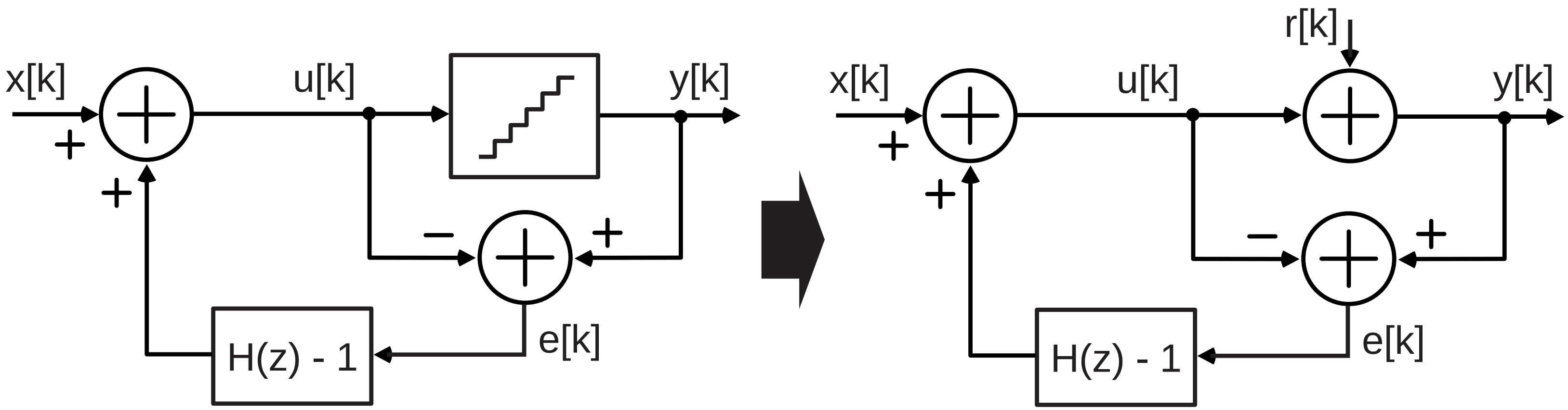


- **Represent quantizer block as a summing junction in which r[k] represents quantization error**
  - **Note:**

$$e[k] = y[k] - u[k] = (u[k] + r[k]) - u[k] = r[k]$$

- **It is assumed that r[k] has statistics similar to white noise**
  - **This is a key assumption for modeling – often not true!**

Calculation of Signal and Noise Transfer Functions



- **Calculate using Z-transform of signals in linearized model**

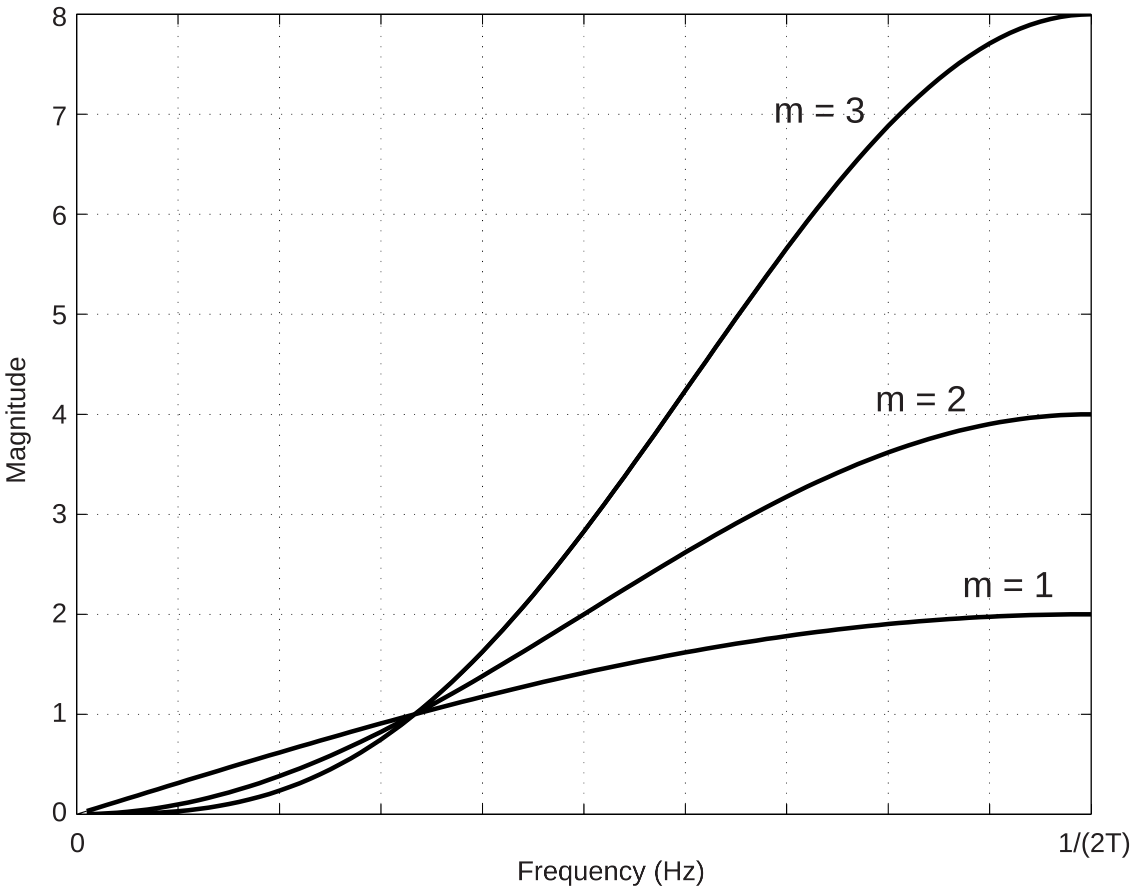
$$\begin{aligned} Y(z) &= U(z) + R(z) \\ &= X(z) + (H(z)-1)E(z) + R(z) \\ &= X(z) + (H(z)-1)R(z) + R(z) \\ &= X(z) + H(z)R(z) \end{aligned}$$

  - **NTF: $H_n(z) = H(z)$**
  - **STF: $H_s(z) = 1$**

A Common Choice for H(z)

$$H(z) = (1 - z^{-1})^m$$

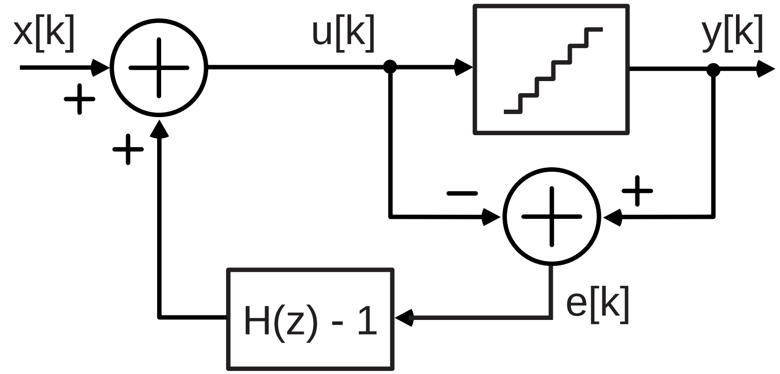
$$\Rightarrow \ |H(e^{j2\pi fT})| = |(1 - e^{-j2\pi fT})^m|$$



Example: First Order Sigma-Delta Modulator

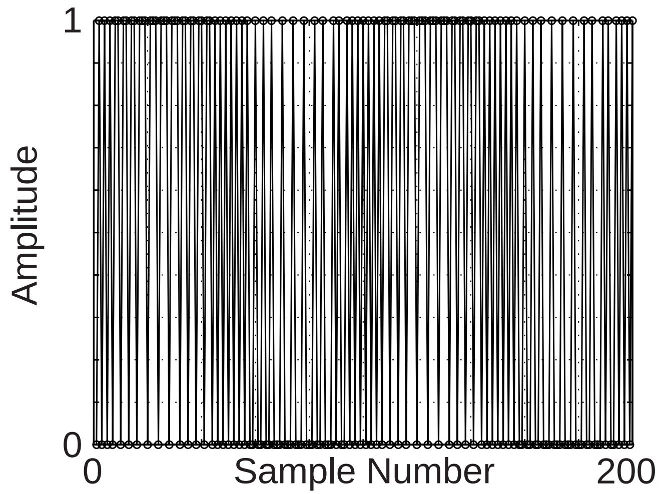
- **Choose NTF to be**

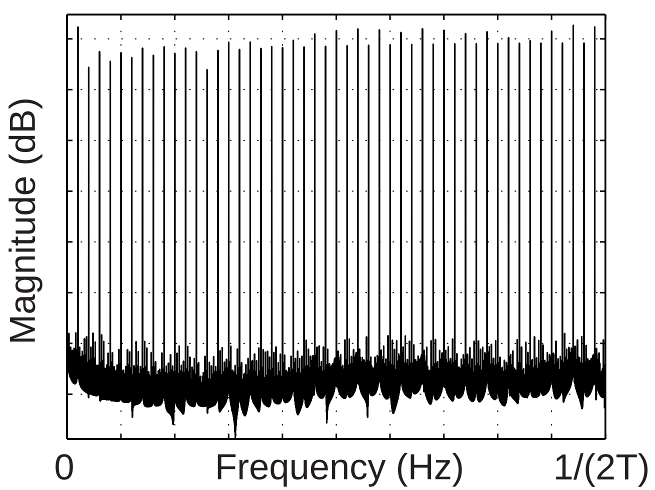
$$H_n(z) = H(z) = 1 - z^{-1}$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$$

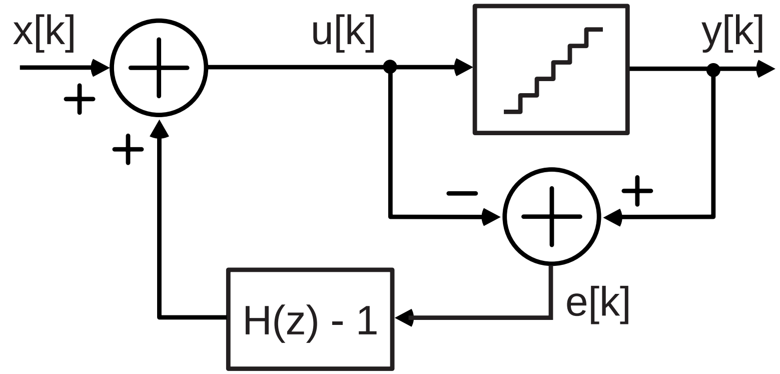




Example: Second Order Sigma-Delta Modulator

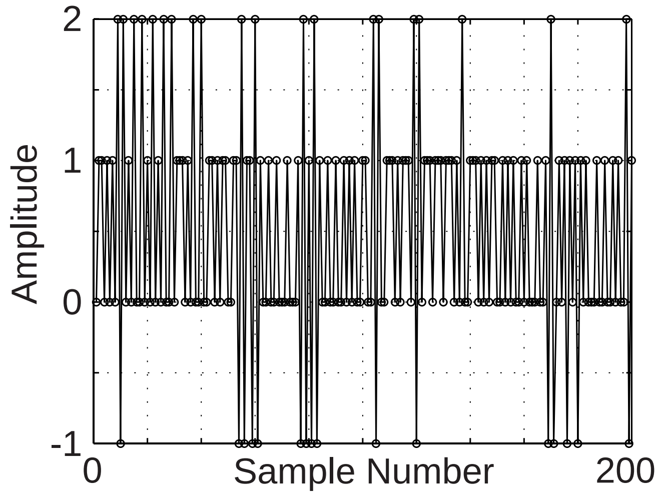
- **Choose NTF to be**

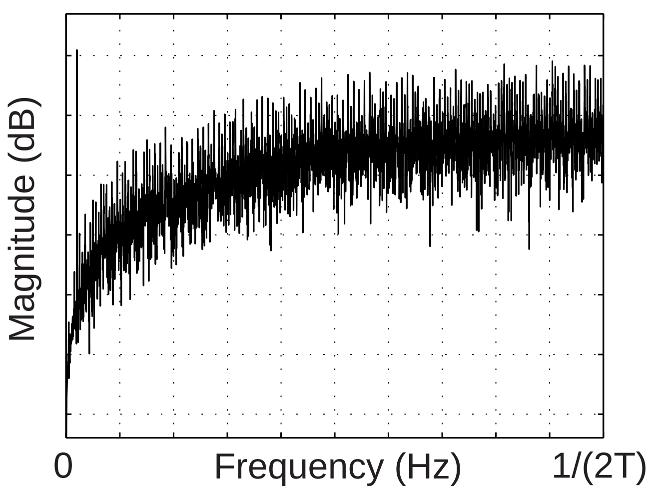
$$H_n(z) = H(z) = (1 - z^{-1})^2$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$$

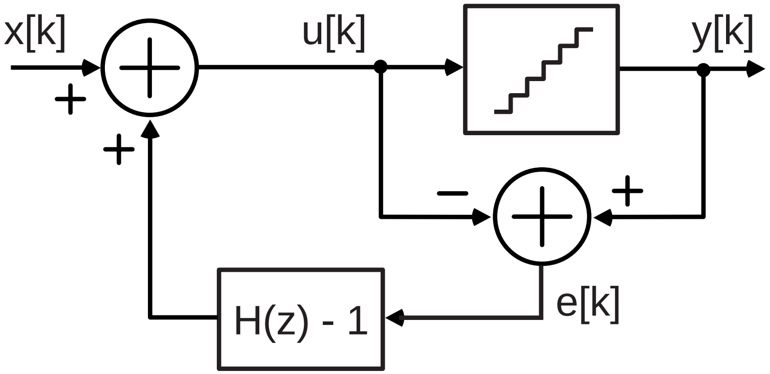




Example: Third Order Sigma-Delta Modulator

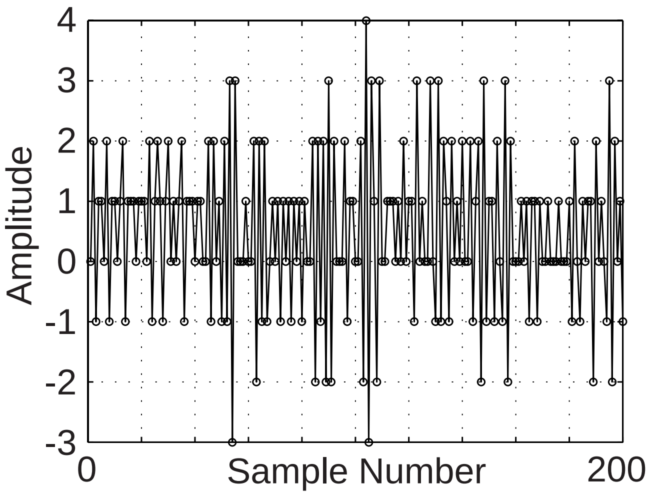
- **Choose NTF to be**

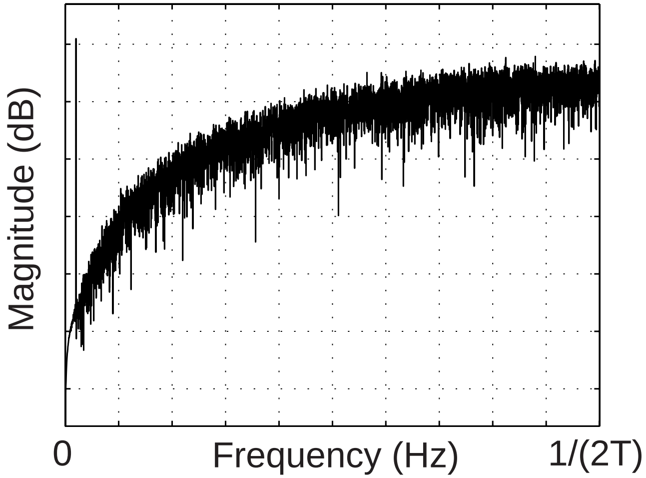
$$H_n(z) = H(z) = (1 - z^{-1})^3$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$$



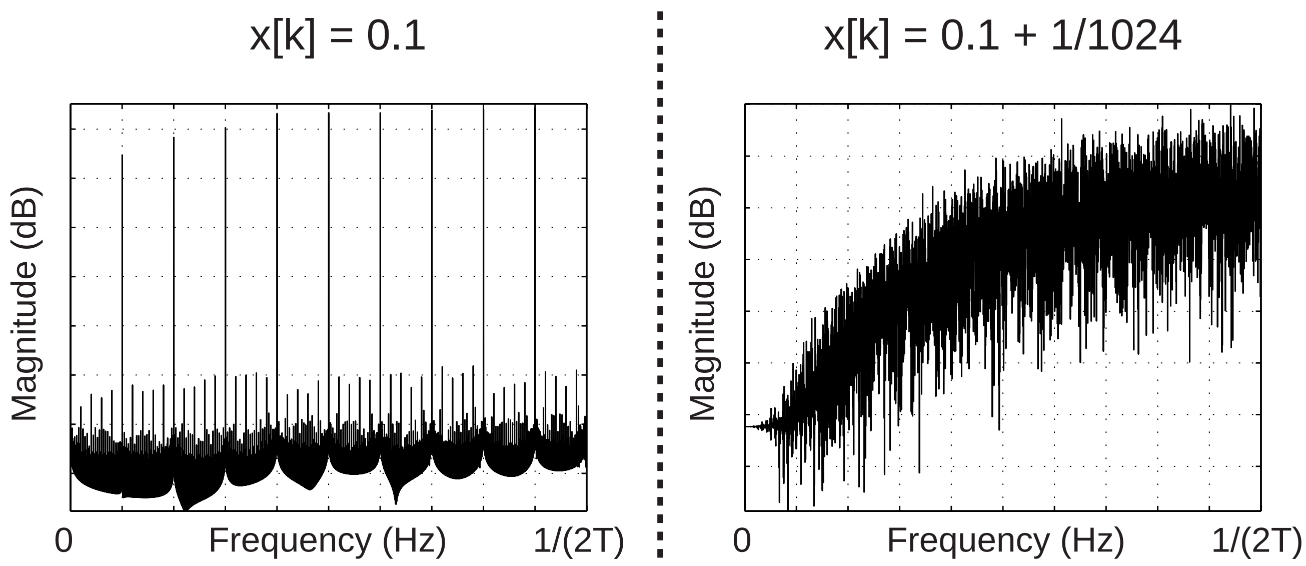


Observations

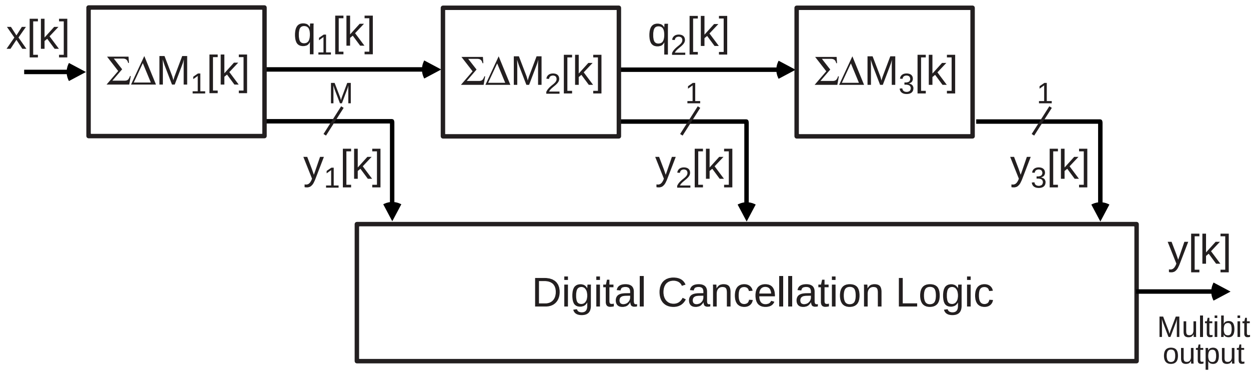
- **Low order Sigma-Delta modulators do not appear to produce "shaped" noise very well**
  - **Reason: low order feedback does not properly "scramble" relationship between input and quantization noise**
    - Quantization noise, r[k], fails to be white
- **Higher order Sigma-Delta modulators provide much better noise shaping with fewer spurs**
  - **Reason: higher order feedback filter provides a much more complex interaction between input and quantization noise**

Warning: Higher Order Modulators May Still Have Tones

- **Quantization noise, r[k], is best whitened when a “sufficiently exciting” input is applied to the modulator**
  - **Varying input and high order helps to “scramble” interaction between input and quantization noise**
- **Worst input for tone generation are DC signals that are rational with a low valued denominator**
  - **Examples (third order modulator):**

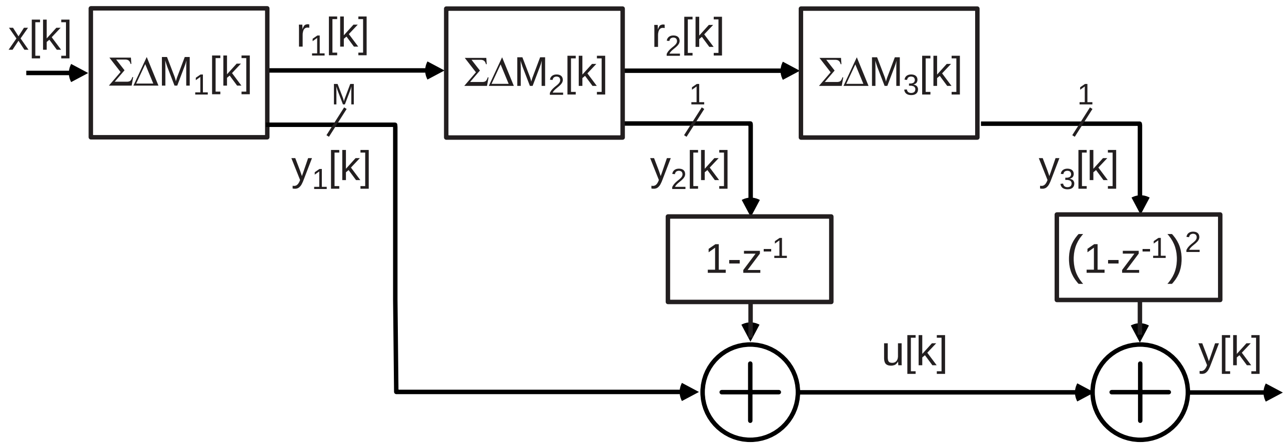


Cascaded Sigma-Delta Modulator Topologies



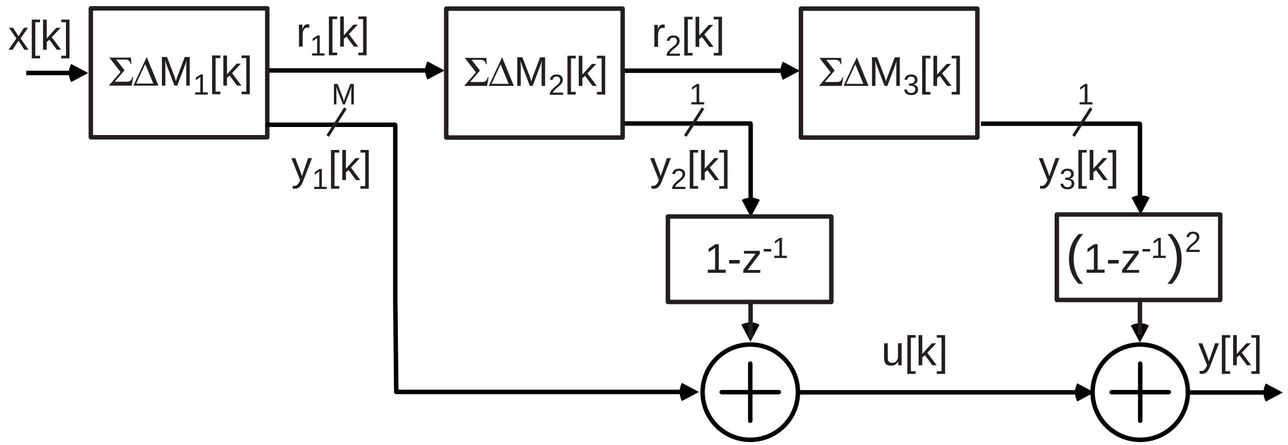
- **Achieve higher order shaping by cascading low order sections and properly combining their outputs**
- **Advantage over single loop approach**
  - **Allows pipelining to be applied to implementation**
    - High speed or low power applications benefit
- **Disadvantages**
  - **Relies on precise matching requirements when combining outputs (not a problem for digital implementations)**
  - **Requires multi-bit quantizer (single loop does not)**

MASH topology



- **Cascade first order sections**
- **Combine their outputs after they have passed through digital differentiators**

Calculation of STF and NTF for MASH topology (Step 1)



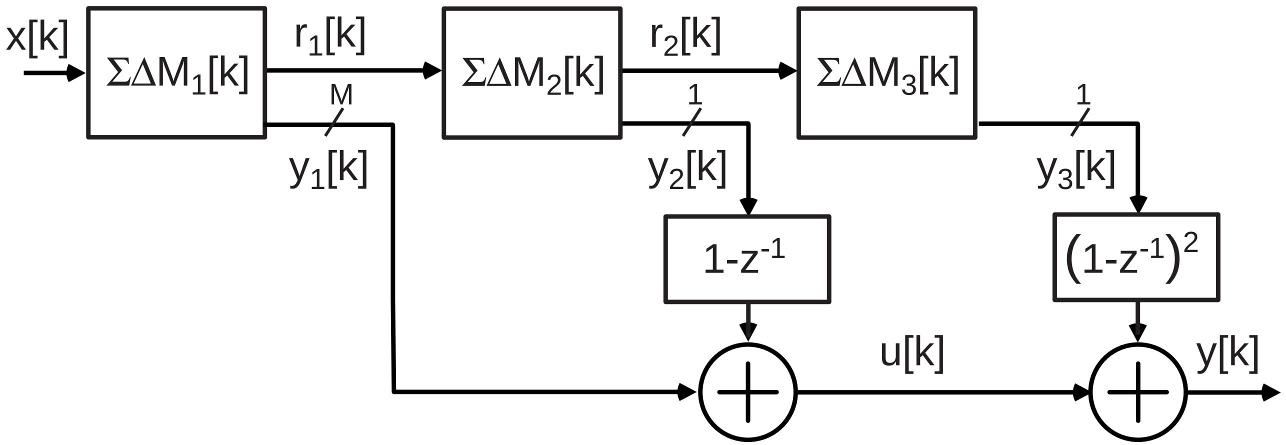
- **Individual output signals of each first order modulator**

$$\begin{aligned} y_1(z) &= x(z) - (1 - z^{-1}) r_1(z) \\ y_2(z) &= r_1(z) - (1 - z^{-1}) r_2(z) \\ y_3(z) &= r_2(z) - (1 - z^{-1}) r_3(z) \end{aligned}$$

- **Addition of filtered outputs**

$$\begin{array}{rr} & y_1(z) \\ + & (1 - z^{-1}) y_2(z) \\ + & (1 - z^{-1})^2 y_2(z) \\ \hline = & x(z) - (1 - z^{-1})^3 r_3(z) \end{array}$$

Calculation of STF and NTF for MASH topology (Step 1)

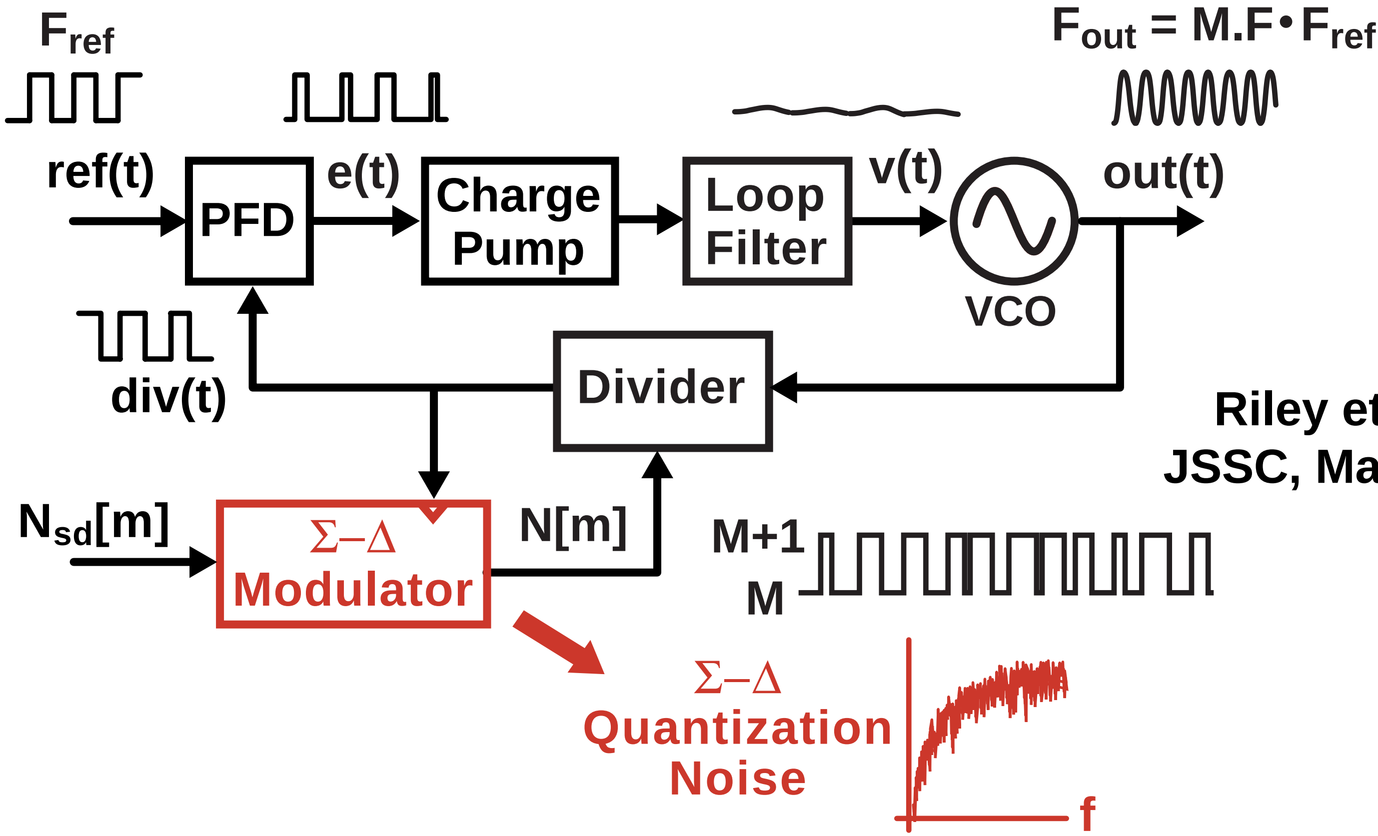


- **Overall modulator behavior**

$$y(z) = x(z) - (1 - z^{-1})^3 r_3(z)$$

  - **STF: $H_s(z) = 1$**
  - **NTF: $H_n(z) = (1 - z^{-1})^3$**

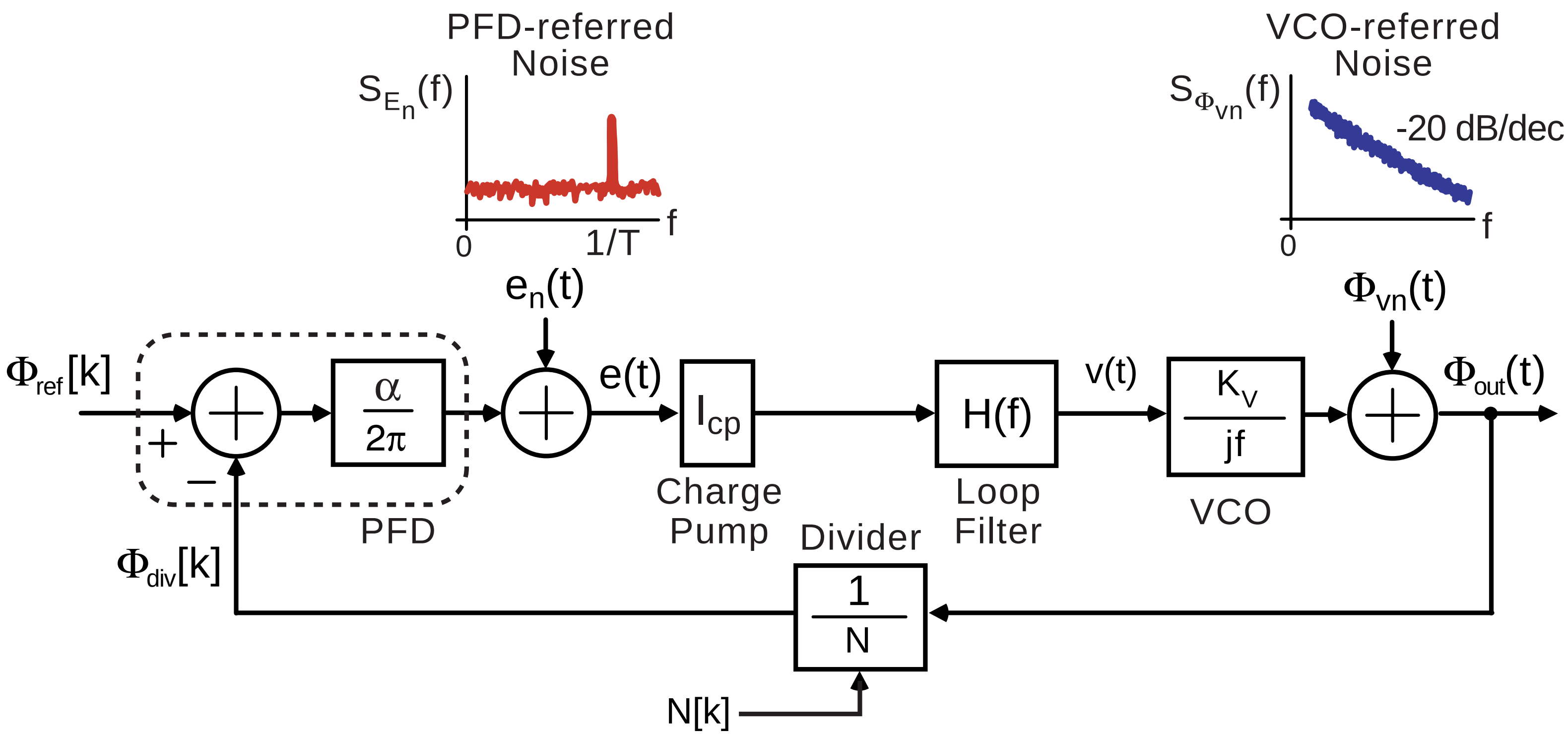
Sigma-Delta Frequency Synthesizers



Riley et. al., JSSC, May 1993

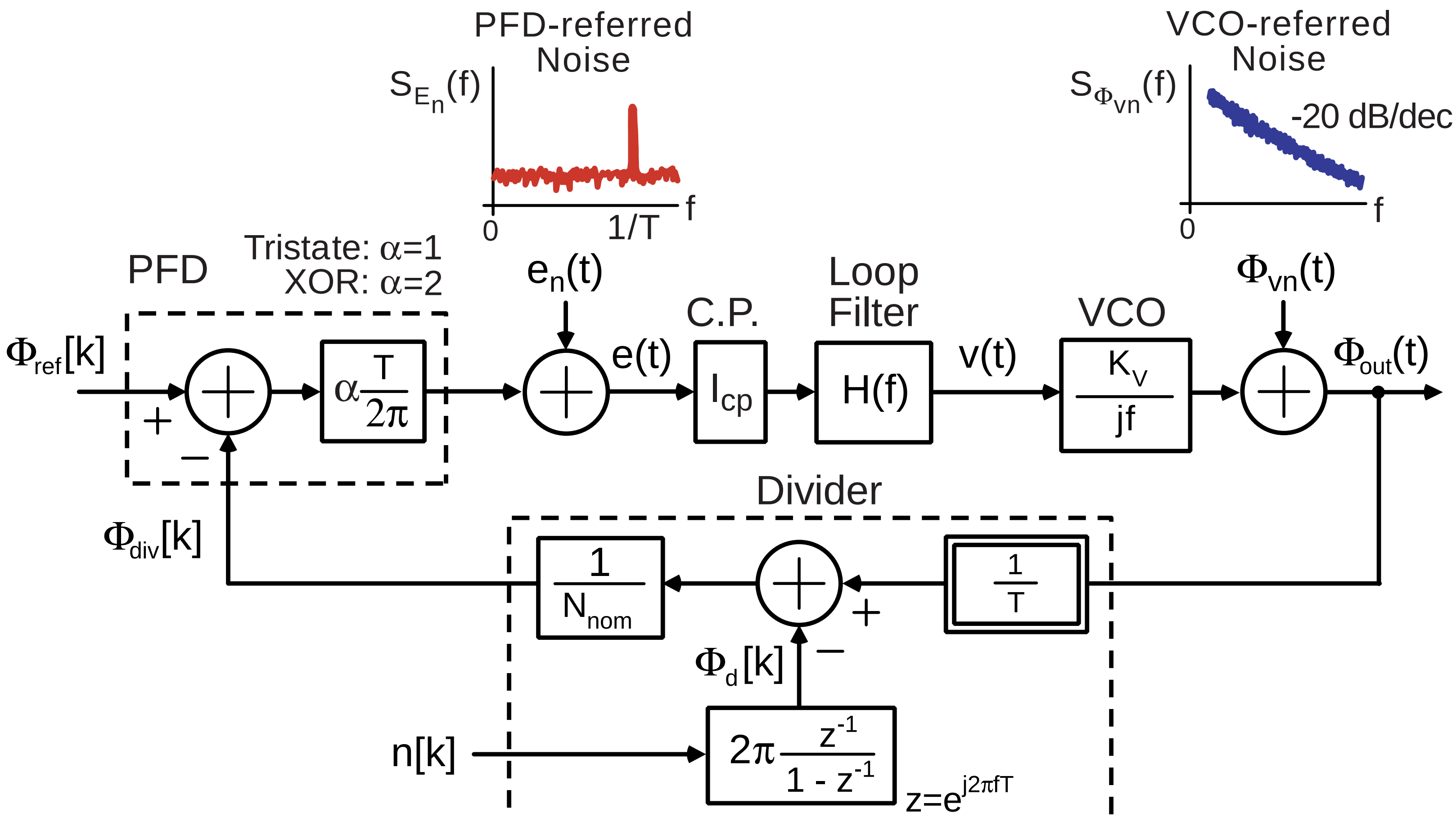
- Use Sigma-Delta modulator rather than accumulator to perform dithering operation
  - Achieves much better spurious performance than classical fractional-N approach

Background: The Need for A Better PLL Model



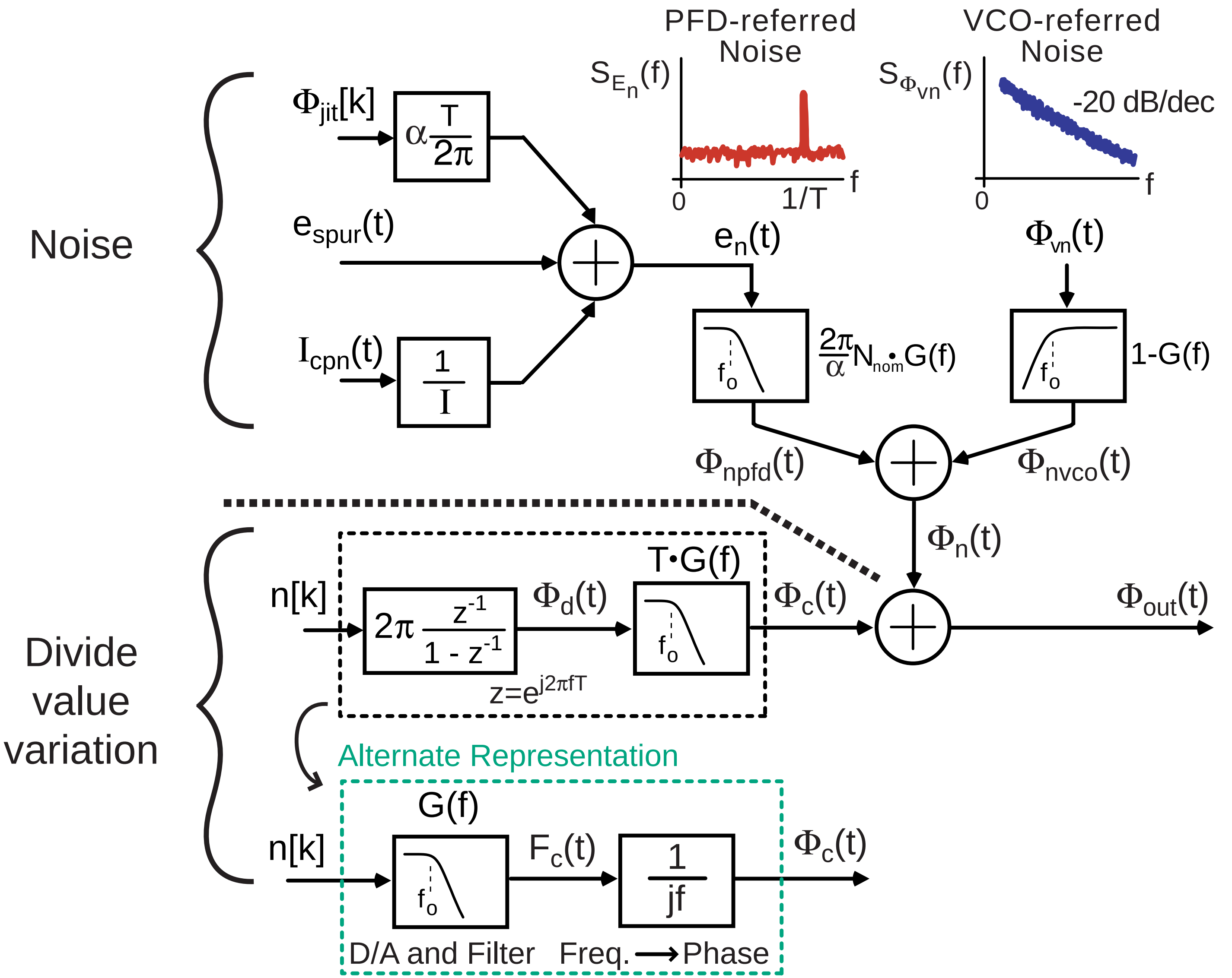
- **Classical PLL model**
  - **Predicts impact of PFD and VCO referred noise sources**
  - **Does not allow straightforward modeling of impact due to divide value variations**
    - This is a problem when using fractional-N approach

A PLL Model Accommodating Divide Value Variations

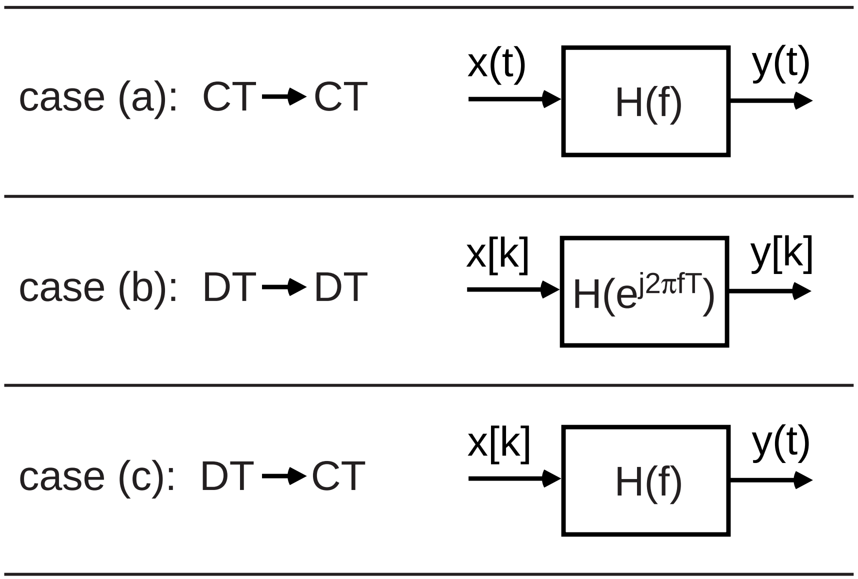


- **See derivation in Perrott et. al., "A Modeling Approach for Sigma-Delta Fractional-N Frequency Synthesizers …", JSSC, Aug 2002**

Parameterized Version of New Model

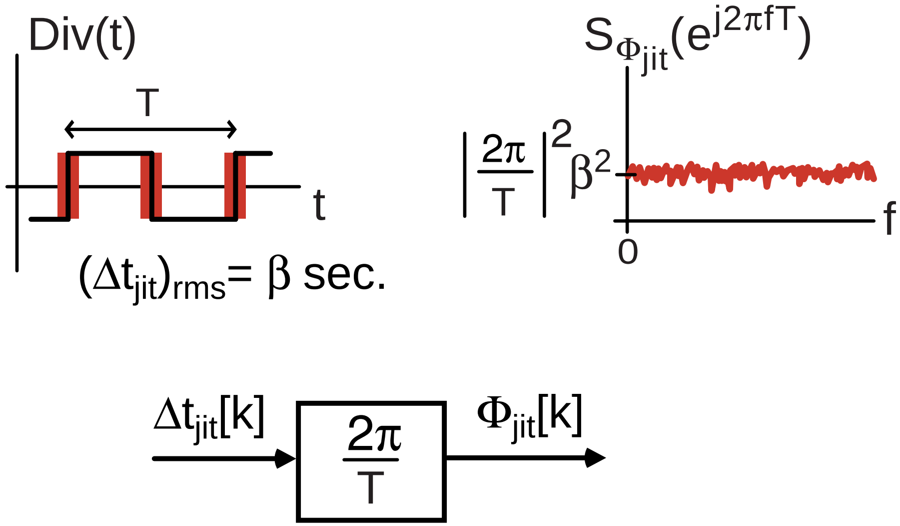


Spectral Density Calculations



- **Case (a):** $$S_y(f) = |H(f)|^2 S_x(f)$$
- **Case (b):** $$S_y(e^{j2\pi fT}) = |H(e^{j2\pi fT})|^2 S_x(e^{j2\pi fT})$$
- **Case (c):** $$S_y(f) = \frac{1}{T}|H(f)|^2 S_x(e^{j2\pi fT})$$

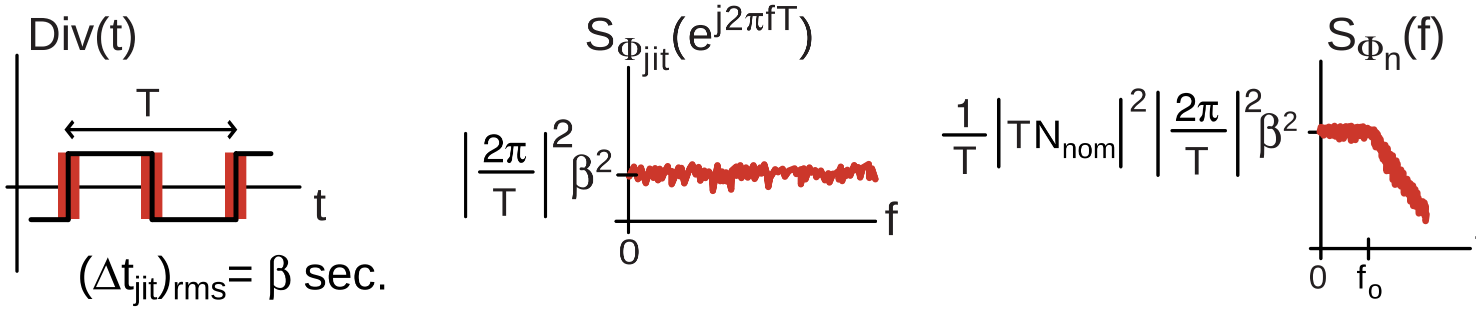
Example: Calculate Impact of Ref/Divider Jitter (Step 1)



- **Assume jitter is white**
  - **i.e., each jitter value independent of values at other time instants**
- **Calculate spectra for discrete-time input and output**
  - **Apply case (b) calculation**

$$S_{\Delta t_{jit}}(e^{j2\pi fT}) = \beta^2 \quad \Rightarrow \quad S_{\Phi_{jit}}(e^{j2\pi fT}) = \left|\frac{2\pi}{T}\right|^2 \beta^2$$

Example: Calculate Impact of Ref/Divider Jitter (Step 2)

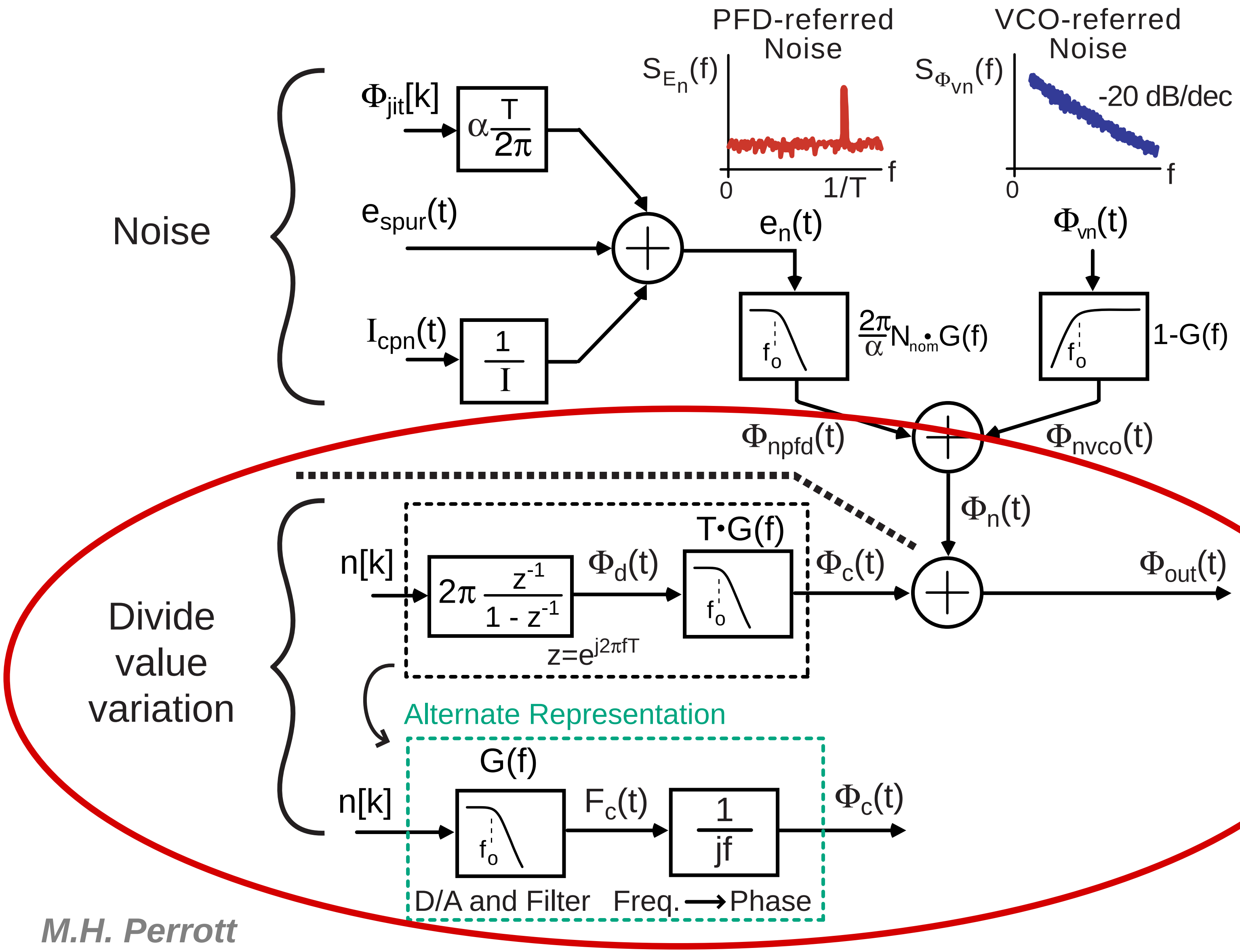


- **Compute impact on output phase noise of synthesizer**
  - **We now apply case (c) calculation**

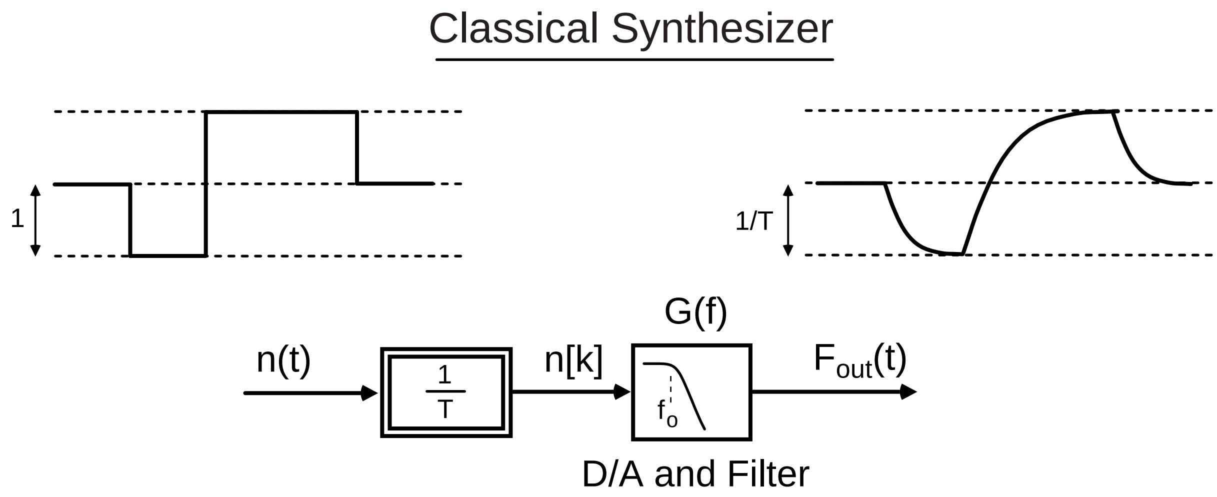
$$S_{\Phi_n}(f) = \frac{1}{T}|TN_{nom}G(f)|^2 S_{\Phi_{jit}}(e^{j2\pi fT})$$
$$= \frac{1}{T}|TN_{nom}G(f)|^2 \left|\frac{2\pi}{T}\right|^2 \beta^2$$

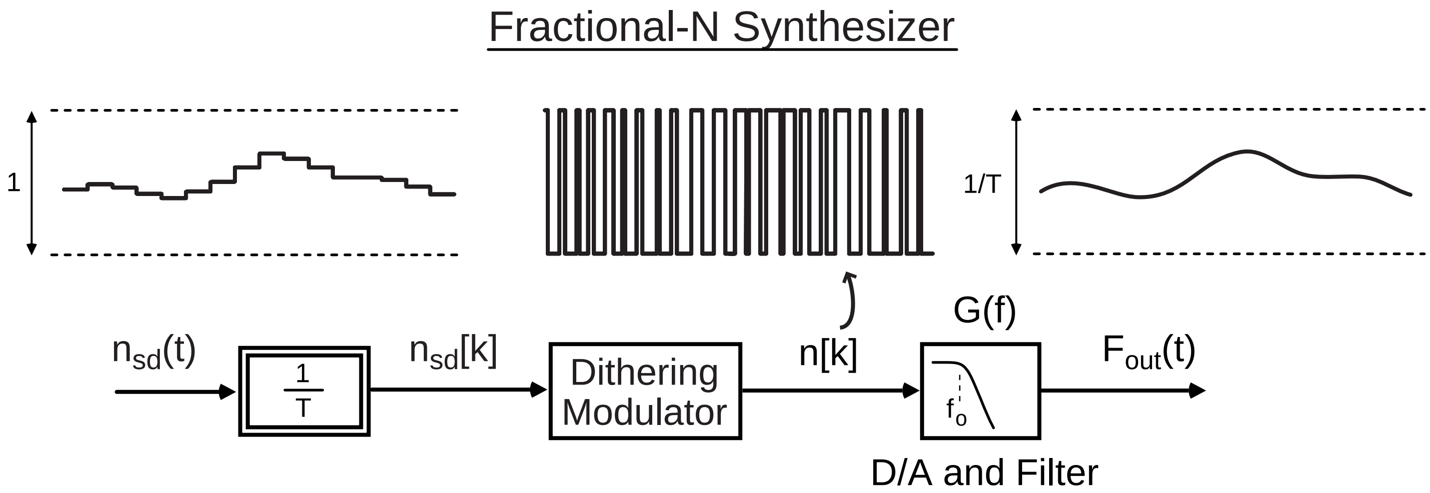
  - **Note that G(f) = 1 at DC**

Now Consider Impact of Divide Value Variations



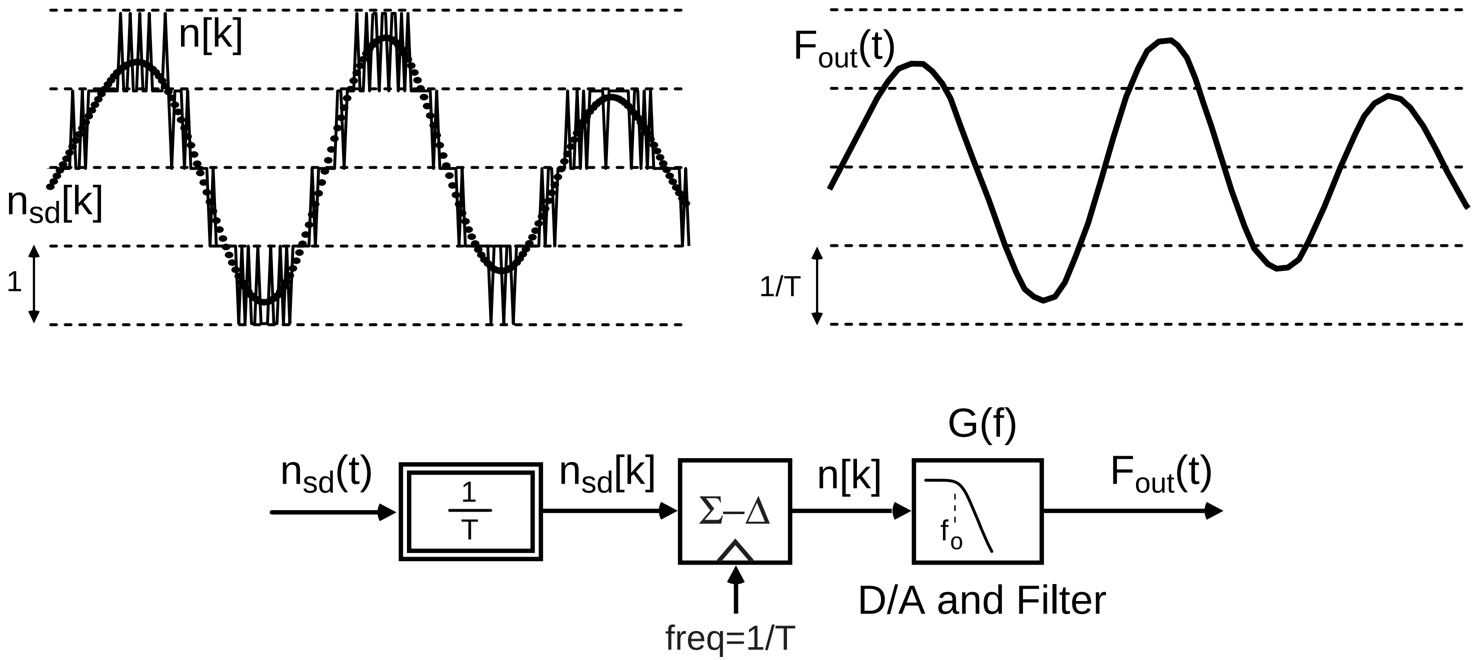
Divider Impact For Classical Vs Fractional-N Approaches





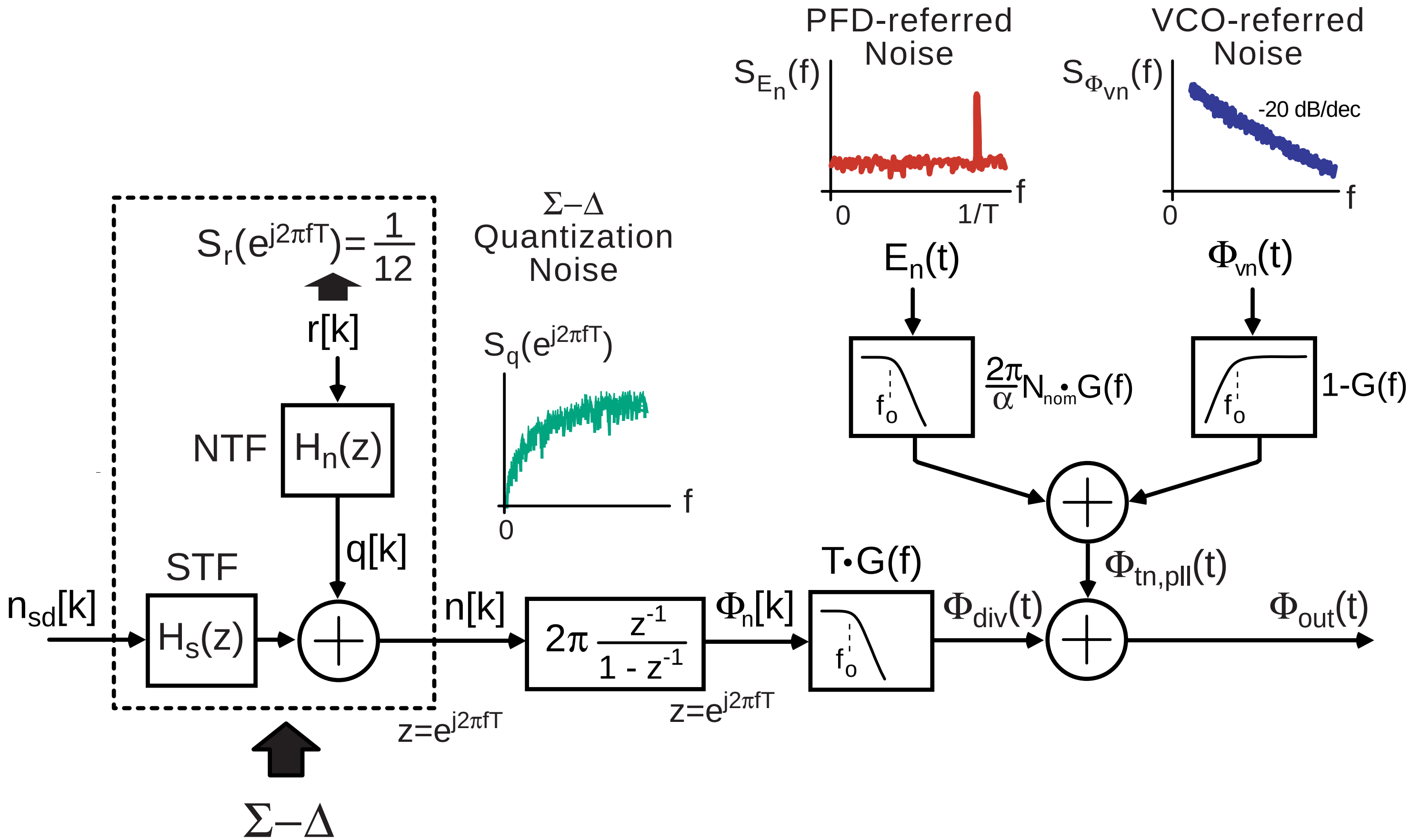
- **Note: 1/T block represents sampler (to go from CT to DT)**

Focus on Sigma-Delta Frequency Synthesizer



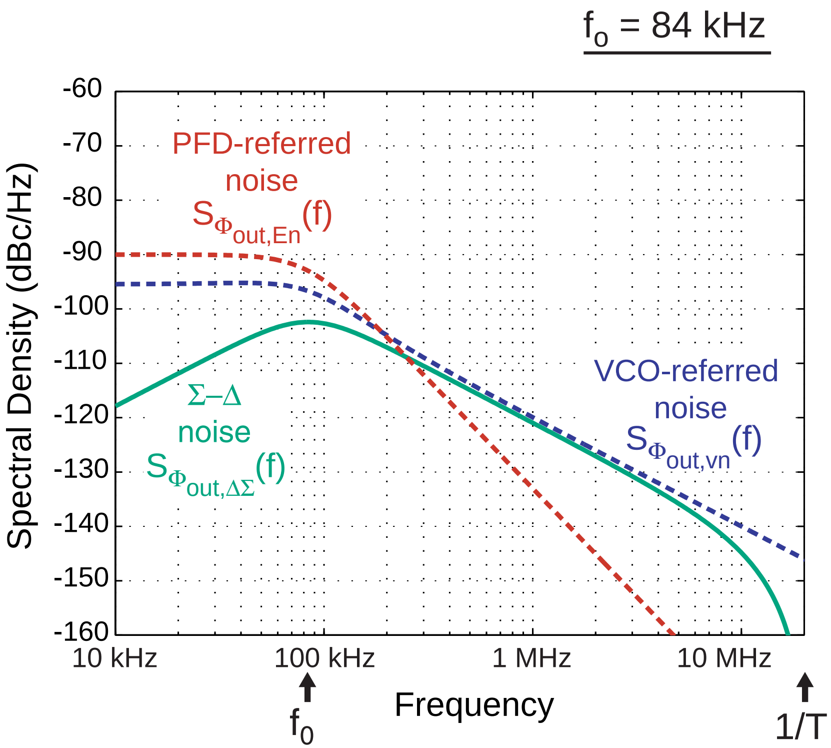
- **Divide value can take on fractional values**
  - **Virtually arbitrary resolution is possible**
- **PLL dynamics act like lowpass filter to remove much of the quantization noise**

Quantifying the Quantization Noise Impact



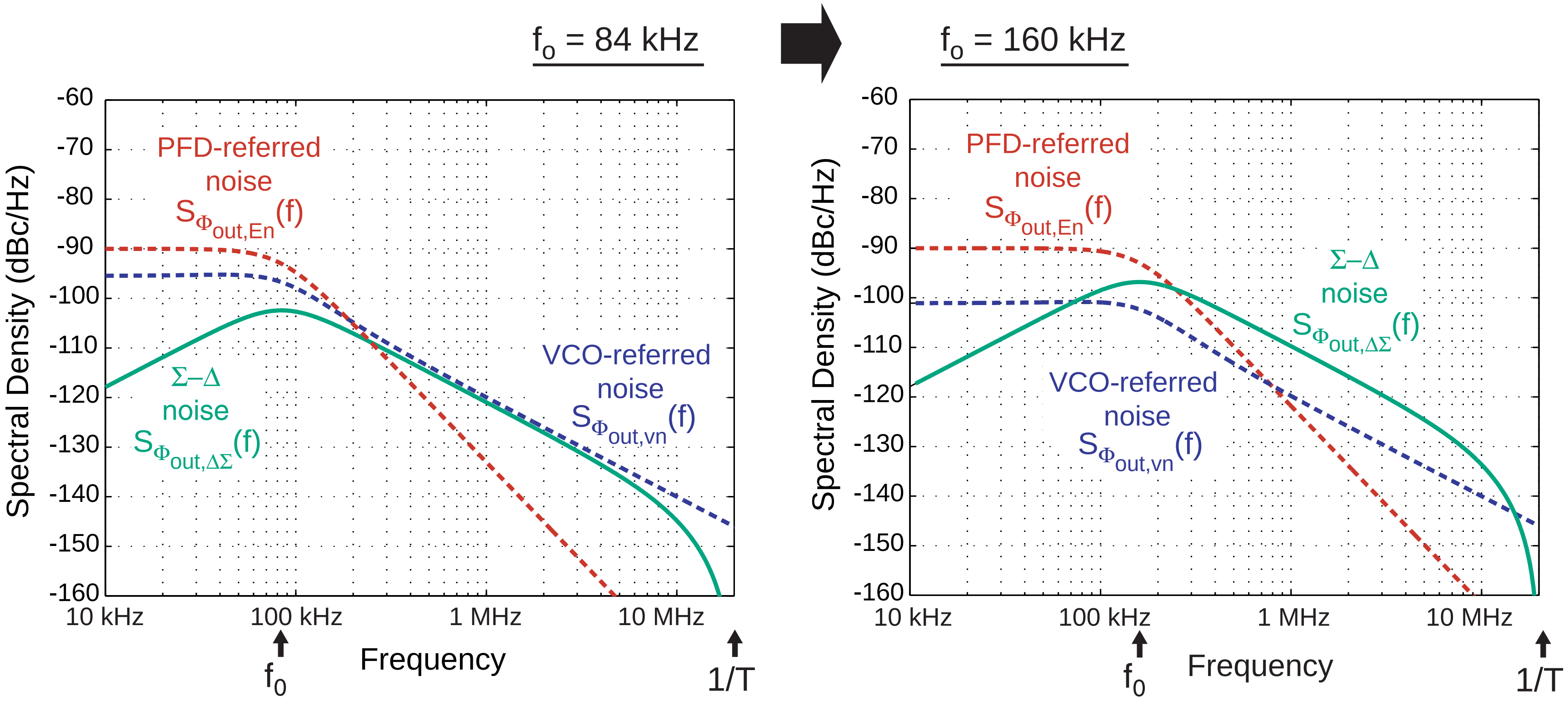
- Calculate by simply attaching Sigma-Delta model
  - We see that quantization noise is integrated and then lowpass filtered before impacting PLL output

A Well Designed Sigma-Delta Synthesizer



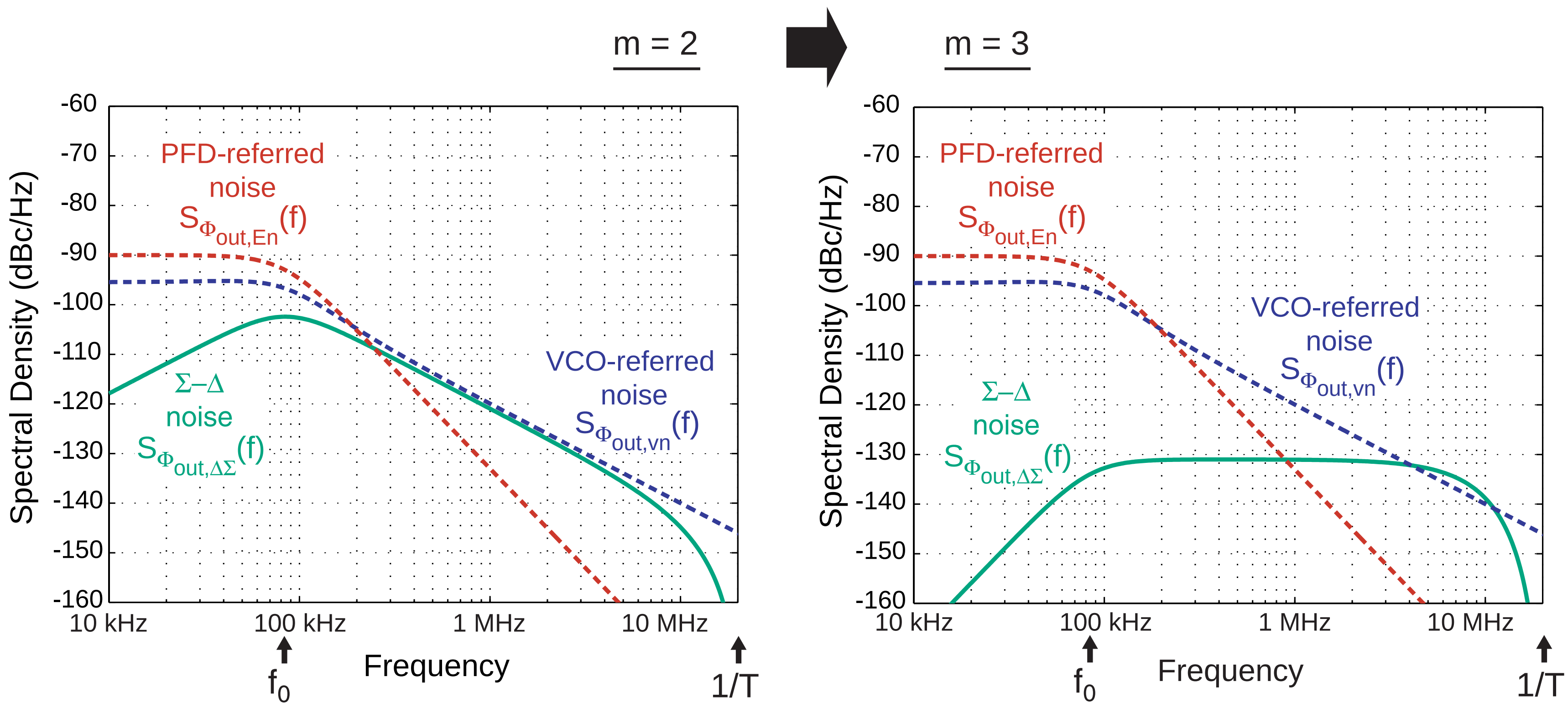
- **Order of G(f) is set to equal to the Sigma-Delta order**
  - **Sigma-Delta noise falls at -20 dB/dec above G(f) bandwidth**
- **Bandwidth of G(f) is set low enough such that synthesizer noise is dominated by intrinsic PFD and VCO noise**

Impact of Increased PLL Bandwidth



- **Allows more PFD noise to pass through**
- **Allows more Sigma-Delta noise to pass through**
- **Increases suppression of VCO noise**

Impact of Increased Sigma-Delta Order



- **PFD and VCO noise unaffected**
- **Sigma-Delta noise no longer attenuated by G(f) such that a -20 dB/dec slope is achieved above its bandwidth**