MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

SINGAPORE-MIT ALLIANCE
Program on Advanced Materials for Micro and Nano Systems

MIT 6.772/SMA 5111: COMPOUND SEMICONDUCTOR DEVICES

Problem Set No. 2 Solutions

Issued: March 4, 2003 **Due:** March 11, 2003

The values used in this problem set are listed in Table 1.

	$Al_{0.40}Ga_{0.60}As$	$GaAs$
$\chi\,[eV]$	3.63	4.07
$E_g\,[eV]$	1.92	1.42
ϵ_r	11.6	12.9
$N_C\ \left[cm^{-3}\right]$	5.0×10^{17}	4.7×10^{17}
$N_V\ \left[cm^{-3}\right]$	8.0×10^{18}	7.0×10^{18}
$\mu_e\ \left[\frac{cm^2}{V \cdot s}\right]$	600	4000
$\mu_h\ \left[\frac{cm^2}{V \cdot s}\right]$	100	400

Table 1: Values used for this problem set

Problem 3.1

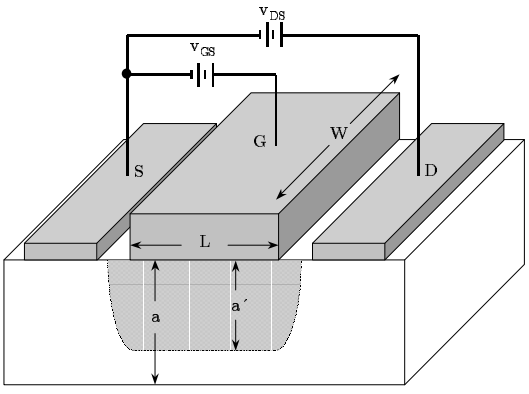

Figure 1: The MESFET

Part a: Design a GaAs MESFET:

The MESFET must be designed such that $a' = a$ when $v_{GS} = 0$.

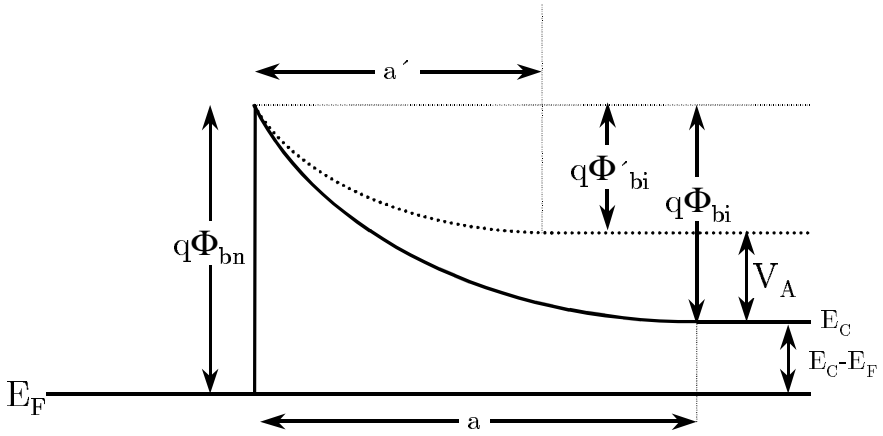

Figure 2: Cross-section of the MESFET.
a: equilibrium depletion depth.
a': Non-equilibrium depletion depth.
$q\Phi_{bn}$: Barrier Height.
$q\Phi_{bi}$: Built-in Potential.
$q\Phi_{bi}'$: Non-Equilibrium Built-in Potential.
V_a: Applied Voltage.

$$
\begin{aligned}
q\Phi_{bn} &= q\Phi_{bi} + (E_C - E_F) = 0.8\ eV \\
E_C - E_F &= \frac{k_B T}{q} ln\left(\frac{N_C}{N_D}\right) \\
&= 39.62\ meV \\
q\Phi_{bi} &= \frac{q^2}{2\epsilon} N_D a^2 = q\Phi_{bn} - (E_C - E_F) \\
a' &= \sqrt{\frac{2\epsilon}{q^2 N_D} q\Phi_{bi}} = \sqrt{\frac{2\epsilon}{q^2 N_D}\left(q\Phi_{bn} - (E_C - E_F)\right)} = 10.41 \times 10^{-6}\ cm \\
a' &= a = 104.19\ nm
\end{aligned}
$$

Part b: What is the maximum conductance, where $v_{GS} = 0.5\ Volts$?

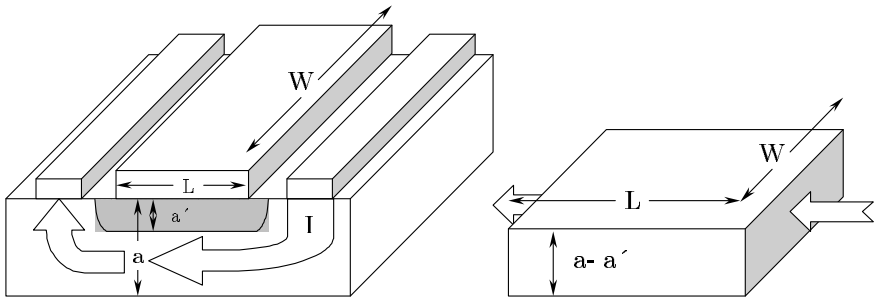

Figure 3: Position and size of the area in question.

Forward biasing will shrink the depletion depth, a'. However, the gate is no longer isolated from the

drain/source channel if $v_{GS} \geq 0.5\ Volts$.

$$\begin{aligned} q\Phi_{bi}' &= \frac{q^2}{2\epsilon} N_D a^2 = q\Phi_{bn} - (E_C - E_F) - qV_A \\ a' &= \sqrt{\frac{2\epsilon}{q^2 N_D} q\Phi_{bi}'} = 6.097 \times 10^{-6}\ cm \\ a - a' &= 4.32 \times 10^{-6}\ cm \\ \sigma &= qn\mu_e + qp\mu_h \cong qn\mu_e \\ G &= \sigma \frac{Area}{Length} = \sigma \frac{(a - a')\, W}{L} = 55.3\ m\mho \end{aligned}$$

Part c:

i: Find the maximum drain current and the corresponding v_{DS}.

The maximum drain current occurs when that the carriers are traveling at the saturation velocity.

$$\begin{aligned} J &= qns_{sat} = 160\ \frac{kAmps}{cm^2} \\ I &= J \cdot A = J \cdot (a - a')\, W = 6.91\ mA \end{aligned}$$

If the field is uniform, then Ohm's law should hold.

$$V = \frac{I}{G} = 125\ mV$$

ii: Is this assumption valid?

If $v_{GS} = 0.5\ V$ and $v_{DS} = 125\ mV$, then $v_{GD} = 375\ mV$. If we evaluate the depletion on both sides of the device, we will find that the depletion width is deeper on the drain side.

$$\begin{aligned} a - a'(V_A = 0.5) &= 43.2\ nm \\ a - a'(V_A = 0.375) &= 30.4\ nm \end{aligned}$$

The channel depth was assumed to be uniform when the saturation current and voltage were calculated. The carriers cannot leave the source with the saturation velocity because they must accelerate as they approach the drain (the cross-sectional area decreases as the carriers approach the drain, so the current density (velocity) must increase in order to maintain current continuity).

Problem 3.2

Part a: Draw the circuit schematic for a direct-coupled FET logic (DCFL) inverter

The circuit schematic is shown in Figure 4.

Part b: Plot the v_{in}/v_{out} transfer characteristic if the output terminal is open circuited

First, v_{in} is limited by metal-semiconductor junction at Q_1. Thus $v_{in} \in [0, 0.8]\ Volts$. Also there should be 4 regions of operation:

1. Q_1 is in cut off region, Q_2 is in triode region
2. Q_1 is in saturation region, Q_2 is in triode region
3. Q_1 is in saturation region, Q_2 is in saturation region
4. Q_1 is in triode region, Q_2 is in saturation region

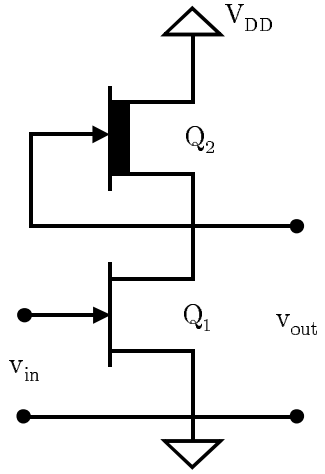

Figure 4: DCFL Inverter

Boundaries between regions:

If Q_1 is in cut off region, $v_{GS1} \in [0, 0.1]\ Volts$ and $I_{D1} = 0\ A$. Since Q_2 is in triode region:

$$\begin{aligned} I_{D2} &= K_2 \left(v_{GS2} - V_{P2} - \frac{v_{DS2}}{2}\right) v_{DS2} \\ &= K_2 \left(-V_{P2} - \frac{v_{DD} - v_{out}}{2}\right) (v_{DD} - v_{out}) = 0 \\ v_{out} &= v_{DD} = 2\ Volts \end{aligned}$$

If Q_2 is in triode region:

$$\begin{aligned} v_{DS2} &< v_{GS2} - V_{P2} \\ v_{DD} - v_{out} &< 0 - (-0.5) \\ v_{out} &> 1.5\ Volts \end{aligned}$$

If Q_1 is in the saturation region:

$$\begin{aligned} v_{DS1} &> v_{GS1} - V_{P1} \\ V_{out} &> V_{in} - 0.1\ Volts \end{aligned}$$

Q_1 is in saturation region, Q_2 is in triode region:

$$\begin{aligned} \frac{K_1}{2} (v_{GS1} - V_{P1})^2 &= K_2 \left(v_{GS2} - V_{P2} - \frac{v_{DS2}}{2}\right) v_{DS2} \\ \frac{K_1}{2} (v_{IN} - V_{P1})^2 &= K_2 \left(-V_{P2} - \frac{v_{DD} - V_{out}}{2}\right) (v_{DD} - V_{out}) \\ 0 &= V_{out}^2 - 3V_{out} + \left(2.01 + V_{IN}^2 - 0.2V_{IN}\right) \\ V_{out} &= 1.5 \pm \sqrt{0.24 - V_{IN}^2 - 0.2V_{IN}} \\ \text{In this region, } V_{out} &> 1.5\ Volts \\ V_{out} &= 1.5 + \sqrt{0.24 - V_{IN}^2 - 0.2V_{IN}} \end{aligned}$$

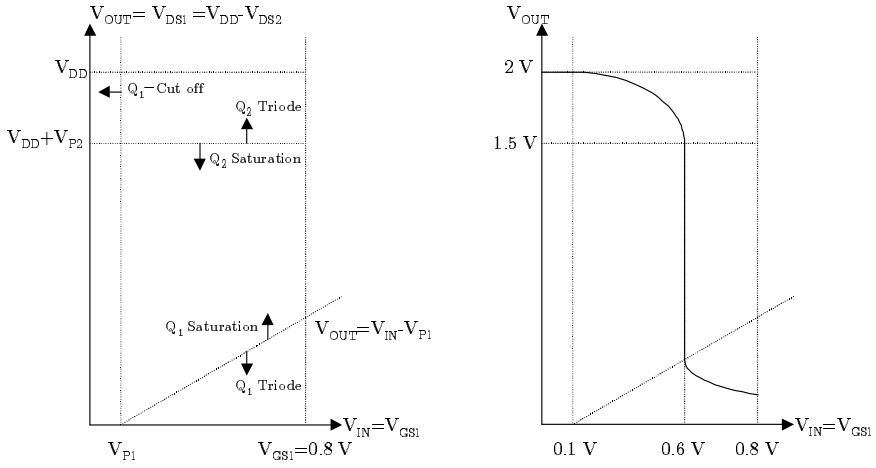

Figure 5: Transfer characteristic of an open circuit DCFL inverter.

Q_1 is in saturation region, Q_2 is in saturation region:

$$\begin{aligned}
\frac{K_1}{2}\left(v_{GS1}-V_{P1}\right)^2 &= \frac{K_2}{2}\left(v_{GS2}-V_{P2}\right)^2 \\
\left(v_{IN}-V_{P1}\right)^2 &= \left(-V_{P2}\right)^2 \\
V_{in} &= V_{P1}-V_{P2} \\
V_{in} &= 0.6\ Volts
\end{aligned}$$

Q_1 is in triode region, Q_2 is in saturation region:

$$\begin{aligned}
\frac{K_2}{2}\left(v_{GS2}-V_{P2}\right)^2 &= K_1\left(v_{GS1}-V_{P1}-\frac{v_{DS1}}{2}\right)v_{DS1} \\
\left(-V_{P2}\right)^2 &= 2\left(V_{in}-V_{P1}-\frac{V_{out}}{2}\right)V_{out} \\
0 &= V_{out}^2-\left(0.2-2V_{in}\right)V_{out}+0.25 \\
V_{out} &= \left(V_{in}-0.1\right)\pm\sqrt{V_{IN}^2-0.2V_{IN}-0.24} \\
\text{In this region, } V_{out} &< V_{in}-V_{P1} \\
V_{out} &= \left(V_{in}-0.1\right)-\sqrt{V_{IN}^2-0.2V_{IN}-0.24}
\end{aligned}$$

Part c: Plot the v_{in}/v_{out} transfer characteristic if the output terminal is connected to another DCFL inverter.

The input terminal of the next terminal is essentially a metal-semiconductor junction. If $V_{in} > 0.8\ Volts$, then the output of the first inverter is pinned at 0.8 volts, as shown in Figure 6. If the output is less than 0.8 volts, the transfer curve should be the same as the previous case.

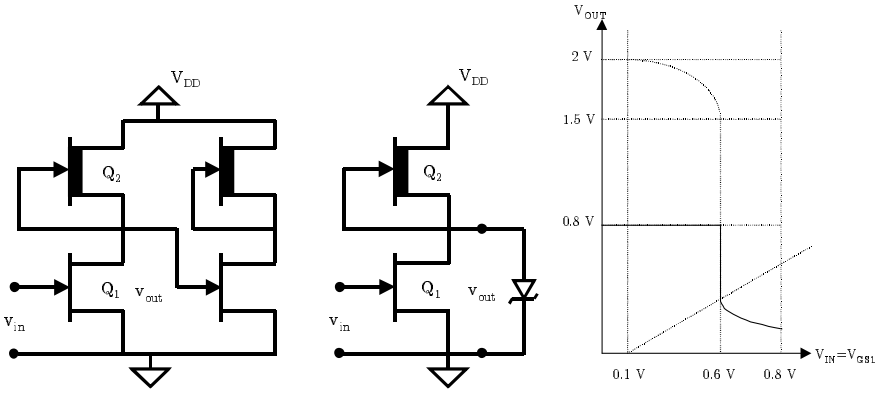

Figure 6:

Problem 3.3

Part a: Calculate the emitter defect of the HBT

$$
\begin{aligned}
\delta_E &= \frac{J_h}{J_e} \\
J_e &= q\frac{n_{po}D_{e,B}}{w_B}\left(e^{-\frac{qV}{k_BT}}-1\right) \\
n_{po} &= \frac{n_{i,base}^2}{N_{A,B}} = \frac{N_{C,B}N_{V,B}e^{-\frac{E_{g,B}}{k_BT}}}{N_{A,B}} \\
J_h &= q\frac{p_{no}D_{h,E}}{w_e}\left(e^{-\frac{qV}{k_BT}}-1\right) \\
p_{no} &= \frac{n_{i,emitter}^2}{N_{D,E}} = \frac{N_{C,E}N_{V,E}e^{-\frac{E_{g,E}}{k_BT}}}{N_{D,E}} \\
\delta_E &= \frac{w_BD_{h,E}N_{A,B}}{w_ED_{e,B}N_{D,E}}\frac{N_{C,B}N_{V,B}}{N_{C,E}N_{V,E}}e^{-\frac{E_{g,E}-E_{g,B}}{k_BT}} \\
&= 9.69\times10^{-8}
\end{aligned}
$$

Part b: Calculate the sheet resistance of the base region

$$
\begin{aligned}
R_\square &= \frac{\rho}{t} = \frac{1}{\sigma\cdot w_B} \\
&= \frac{1}{q\mu_{h,B}N_{A,B}w_B} \\
&= 312.5\frac{\Omega}{square}
\end{aligned}
$$

Part c: Calculate the depletion capacitance between the collector/base junction.

$$\begin{aligned}
\phi_{bi,BC} &= k_B T \cdot ln\left(\frac{N_{A,B} N_{D,C}}{n_{i,B}^2}\right) = 1.371\ eV \\
x_{D,B} &= \sqrt{\frac{2N_{D,C}\epsilon_B\left(\phi_{bi} - qV_A\right)}{q^2 N_{A,B}\left(N_{A,B} + N_{D,C}\right)}} = 1.546\ nm \\
x_{D,C} &= \frac{N_{A,B}}{N_{D,C}} x_{D,B} = 309.285\ nm \\
C' &= \frac{\epsilon_B}{w_D} = \frac{\epsilon_B}{x_{D,B} + x_{D,C}} = 36.75\ \frac{nF}{cm^2}
\end{aligned}$$

Part d: Calculate the base transit time.

$$\tau = \frac{w_B^2}{2D_{e,B}} = 122.07\ fs$$