Lecture 24 - The Si surface and the Metal-Oxide-Semiconductor Structure *(cont.)*

The "Long" Metal-Oxide-Semiconductor Field-Effect Transistor

April 6, 2007

Contents:

1. Dynamics of the MOS structure *(cont.)*
2. Three-terminal MOS structure
3. Introduction to MOSFET

Reading assignment:

del Alamo, Ch. 8, §§8.5-8.6; Ch. 9, §9.1

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Key questions

- What happens to the C-V characteristics of a MOS structure if the *bias* is switched abruptly?
- What happens to the electrostatics of the MOS structure if we contact the inversion layer and we apply a bias to it?
- How does a MOSFET look like and how does it work (roughly)?

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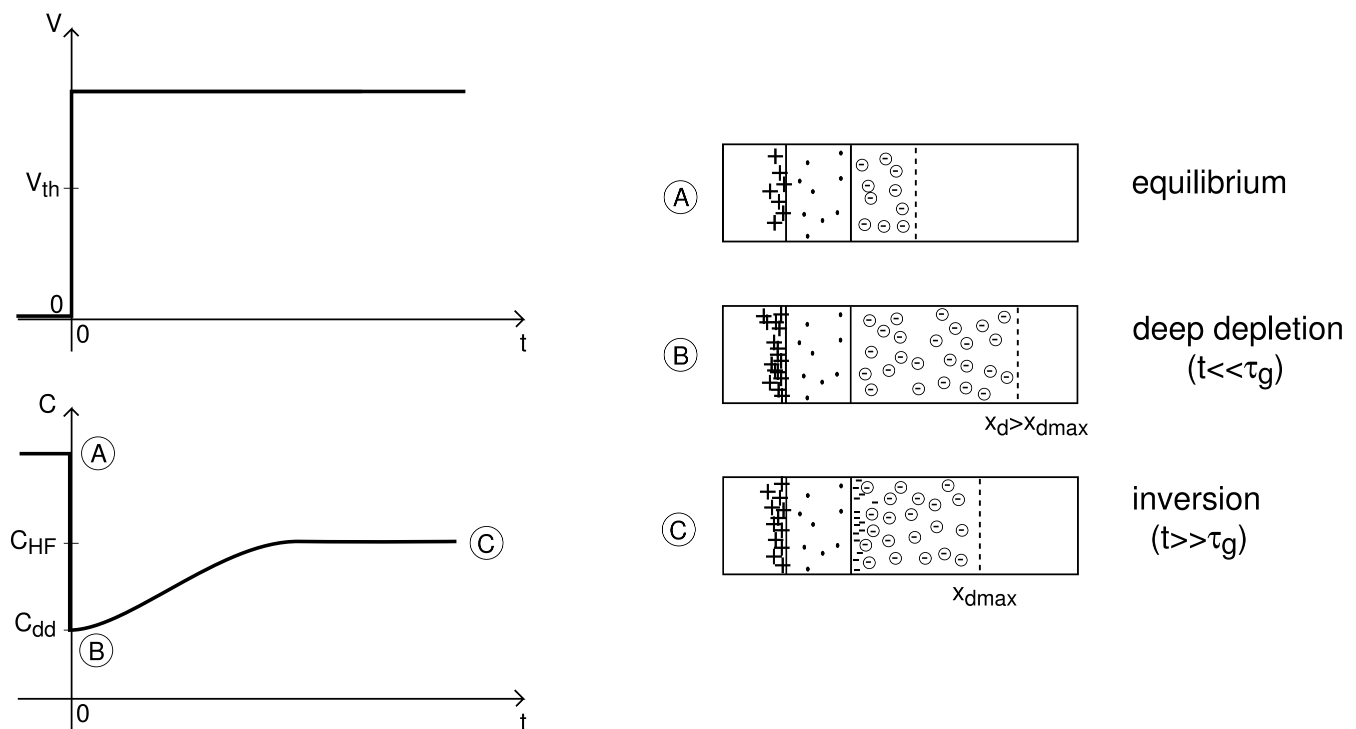
1. Dynamics of the MOS structure *(cont.)*

□ Deep depletion

Consider what happens after the application of a voltage step from depletion towards inversion.

On top of step, put HF small signal to measure C



Immediately after the onset of the step (after an RC delay), inversion layer does not have a chance to grow (electrons must be generated)

→ MOS remains in depletion ("*deep depletion*")

→ x_d grows beyond x_{dmax}

→ C smaller than C_{HF}

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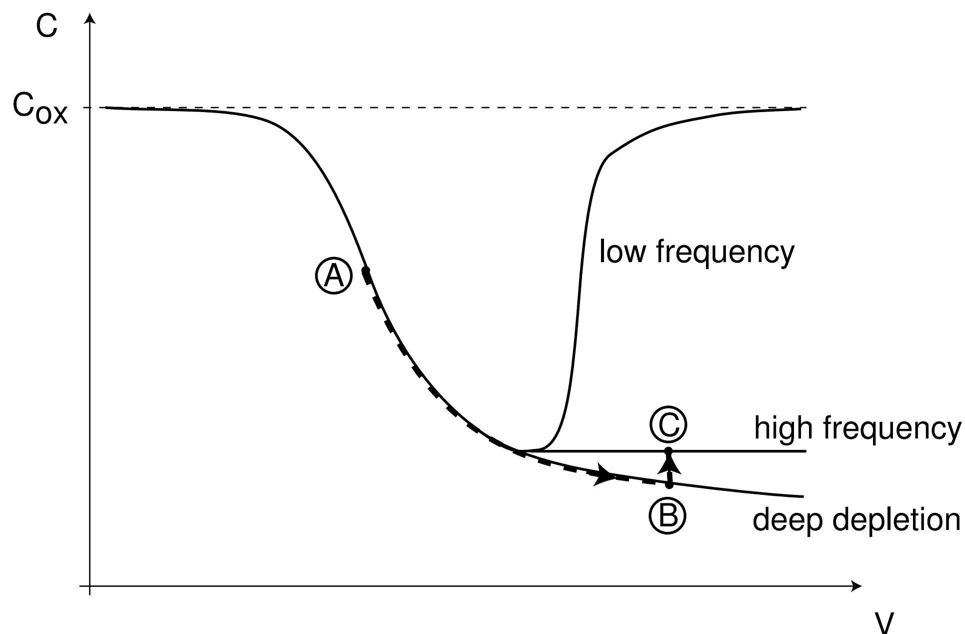
Even though $V > V_{th}$, capacitance in deep depletion described by expression derived for depletion regime:

$$C_{dd} \simeq \frac{C_{ox}}{\sqrt{1 + 4\frac{V - V_{FB}}{\gamma^2}}}$$

C-V characteristics:



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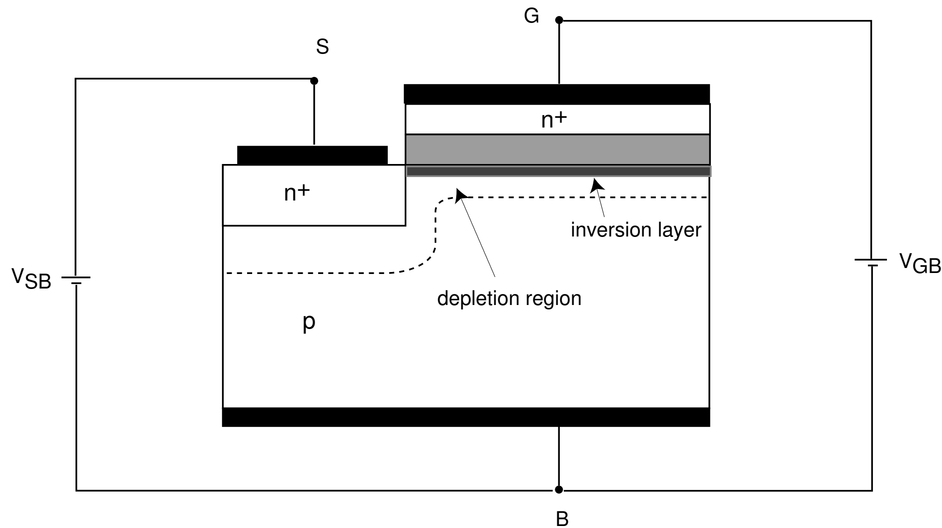
2. Three-terminal MOS structure

Introduce contact to inversion layer:



Can now apply bias to inversion layer with respect to substrate, V_{SB}.

Source-body junction: n$^+$-p junction → only reverse bias desired, $V_{SB} \geq 0$.

Interested only in inversion regime: apply $V_{SB} \geq 0$ keeping V_{GB} constant.

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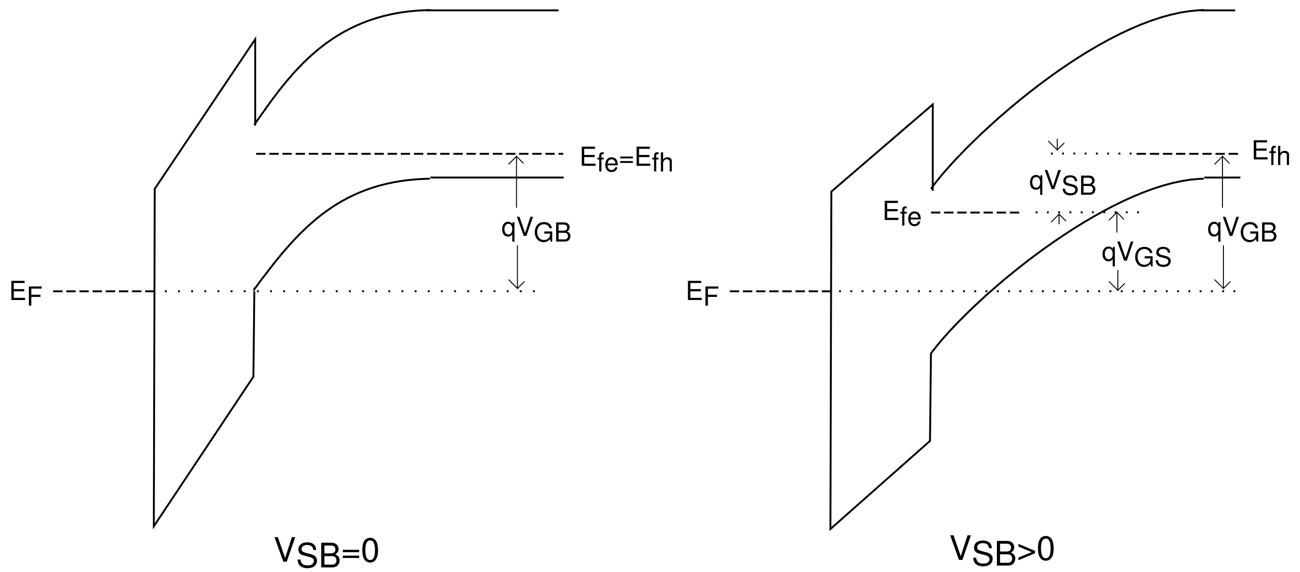
Energy band diagrams:



$$\phi_s(V_{SB}) = \phi_s(V_{SB} = 0) + V_{SB}$$

Application of $V_{SB} > 0$, increases ϕ_s, and also $|Q_d|$.

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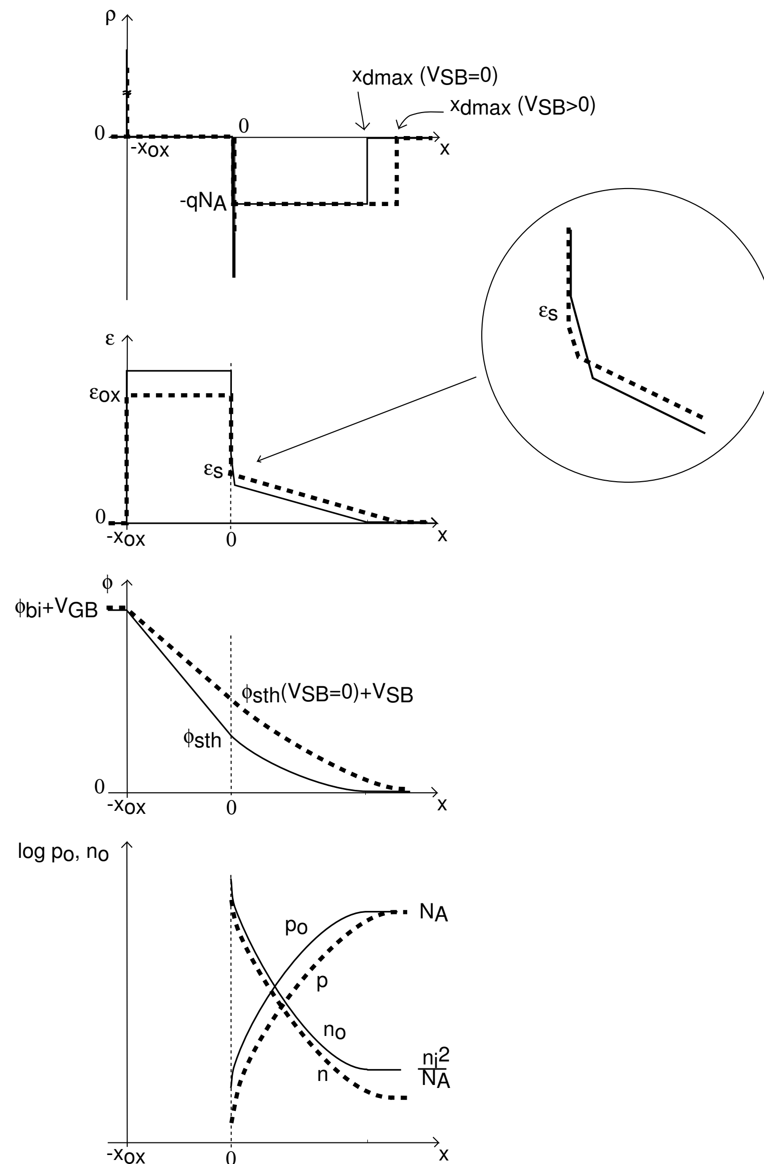
$V_{SB} > 0 \Rightarrow x_d \uparrow \; |Q_d| \uparrow \; \phi_s \uparrow$ (as in reverse bias p-n junction).



Total potential difference from G to B fixed:

$$\phi_{bi} + V_{GB} = \phi_{ox} + \phi_s$$

Hence: $\phi_{ox} \downarrow \Rightarrow \mathcal{E}_{ox} \downarrow \; \mathcal{E}_s \downarrow$

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But:

$$\mathcal{E}_s = -\frac{Q_s}{\epsilon_s}$$

Hence: $|Q_s| \downarrow$

In summary:

$$|Q_s| \downarrow \;\; |Q_d| \uparrow \Rightarrow \;\; |Q_i| \downarrow$$

equivalent to V_{th} shifting positive.

Key conclusion: *application of a body bias turns inversion layer off!*

Important implications for device and circuit design and operation.

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• V_{th} model that accounts for body bias

Go to Poisson-Boltzmann formulation and change:

$$\phi_{sth} \rightarrow \ \phi_{sth} + V_{SB}$$

Then:

$$V_{th} = V_{FB} + \phi_{sth} + V_{SB} + \gamma\sqrt{\phi_{sth} + V_{SB}}$$

For MOSFET operation, interested in threshold in V_{GS}:

$$V_{GB} = V_{GS} + V_{SB}$$

Then:

$$V_{th}^{GS}(V_{SB}) = V_{th}^{GB} - V_{SB} = V_{FB} + \phi_{sth} + \gamma\sqrt{\phi_{sth} + V_{SB}}$$

Can easily rewrite as:

$$V_{th}^{GS}(V_{SB}) = V_{th}^{GS}(V_{SB} = 0) + \gamma(\sqrt{\phi_{sth} + V_{SB}} - \sqrt{\phi_{sth}})$$

Note: $V_{SB} \uparrow \Rightarrow V_{th}^{GS} \uparrow$

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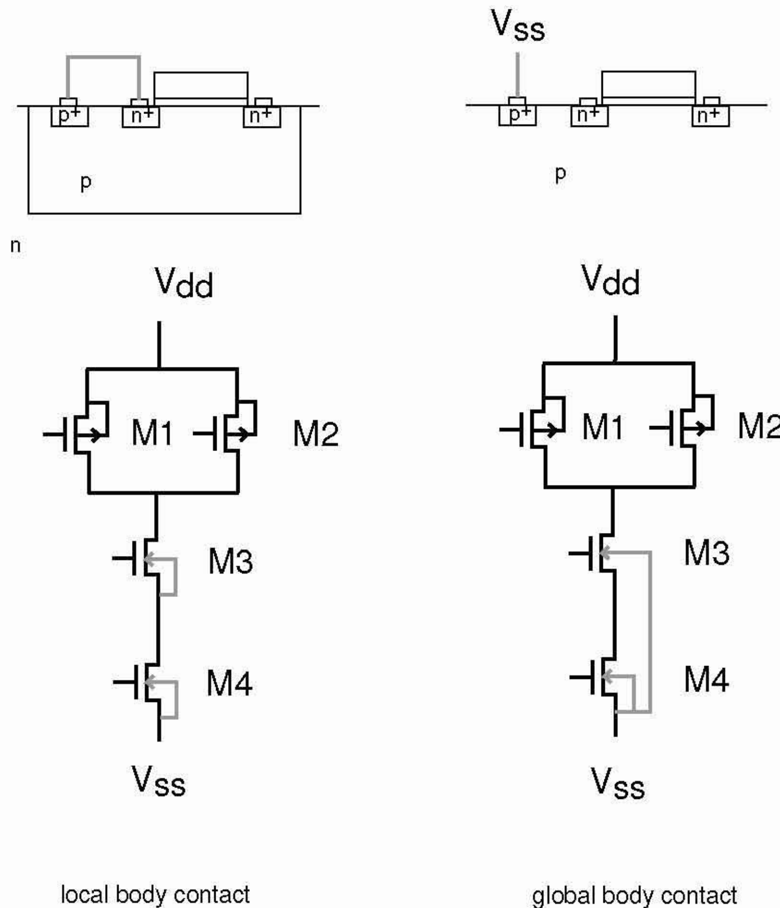
Back bias effect important in MOSFETs and CMOS.

Ideally, the body of every MOSFET should be tied to its source, but that's expensive. What are the trade-offs?



local body contact

global body contact

Focus on M3 (nMOSFET) of NAND gate:

- with local body contact: $V_{SB} = 0$ always $\Rightarrow$ V_{th} predictable
- with global body contact: sometimes $V_{SB} > 0$ $\Rightarrow$ slower switching, *"jitter"*

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3. MOSFET Introduction

Cross section and layout of n-channel MOSFET (NMOS):

body source polysilicon gate drain gate n^+ p^+ n^+ n^+ p inversion layer channel gate oxide n

n p^+ p n^+ n^+ n^+

Inversion layer links source and drain underneath gate.

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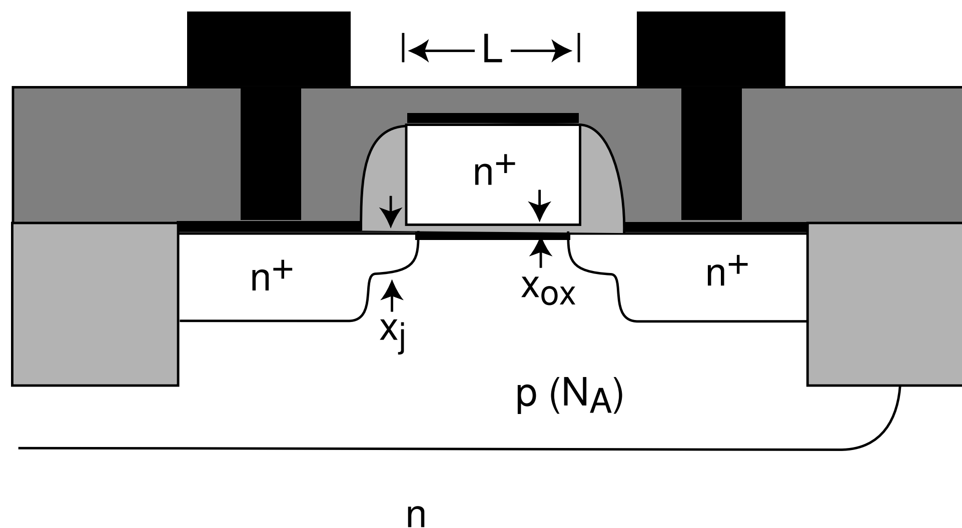
Inversion layer current depends on:

- lateral field across inversion layer (set to first order by drain-to-source voltage)
- electron concentration in inversion layer (set to first order by gate-to-source voltage)



Key design parameters:

- gate length, $L \simeq$ electrical channel length
- gate oxide thickness, x_{ox}
- source and drain junction depth, x_j
- doping level in body, N_A

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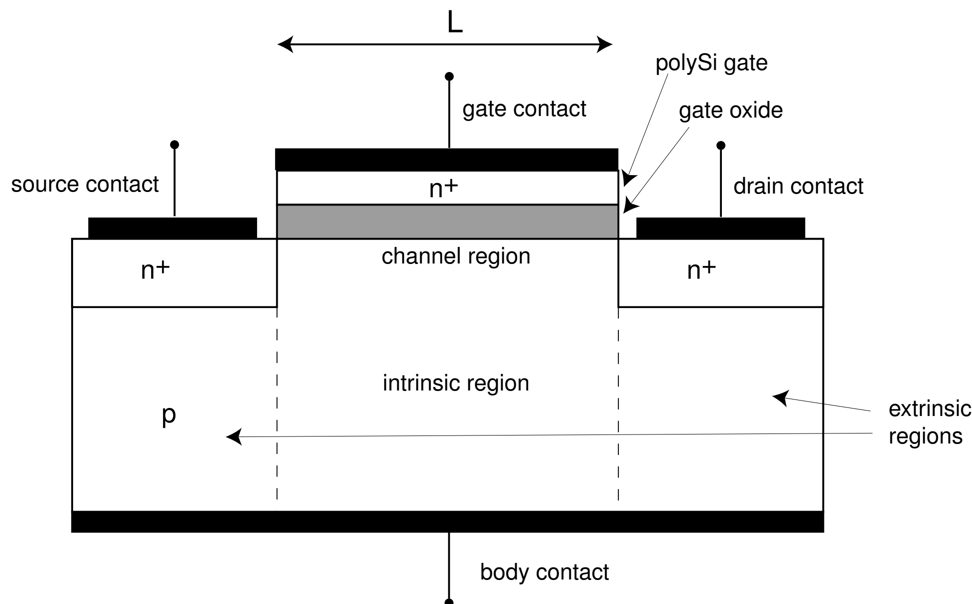
4. The ideal MOSFET



Simplifying assumptions:

- Carrier flow is one dimensional.
- Uniform doping levels
- Electron transport in inversion layer takes place by drift (*i.e.*, neglect diffusion).
- Electrons drift along the inversion layer in the mobility regime, *i.e.*, the electron velocity is proportional to the lateral electric field along the inversion layer.
- Neglect *body effect* (dependence of V_T with y)
- No parasitic resistances

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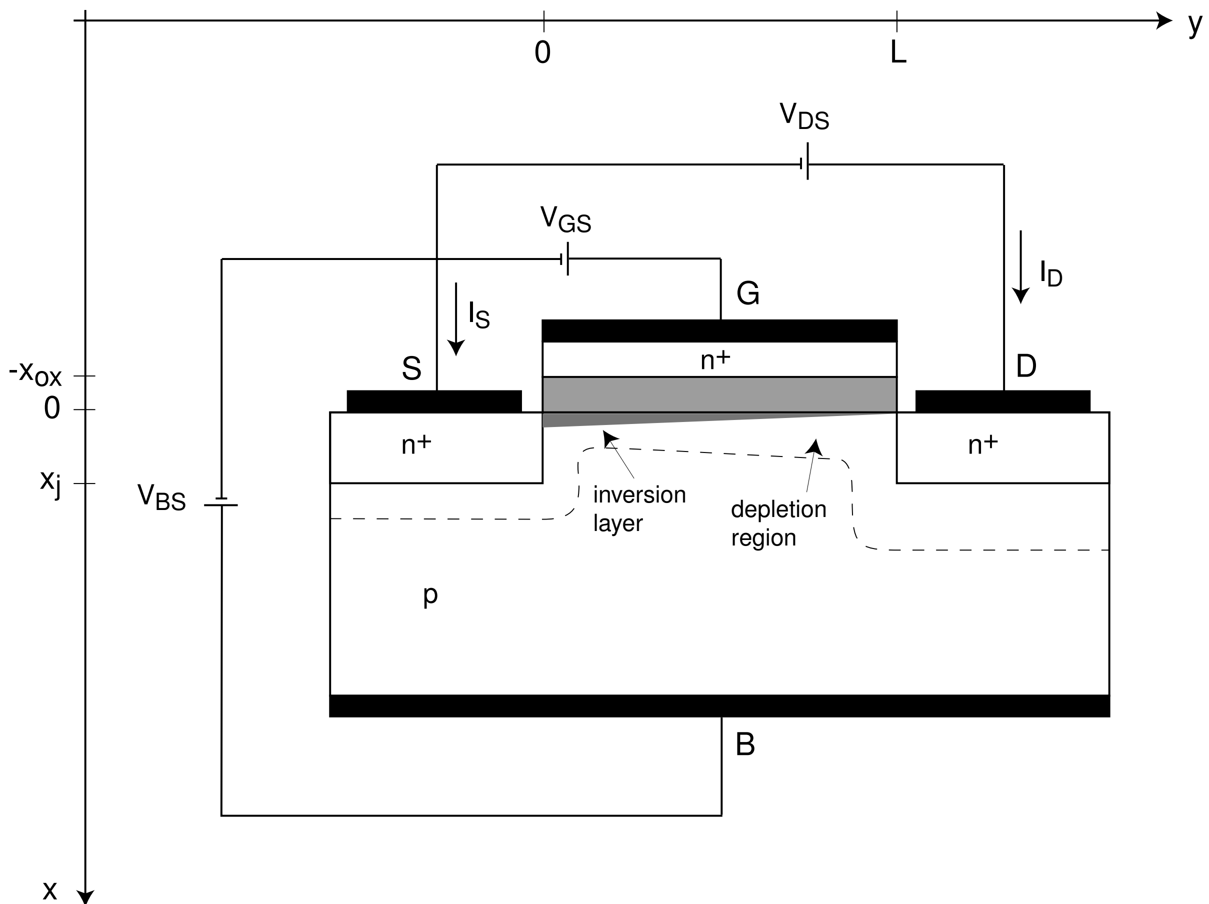
- Ignore junction sidewall effects.
- No three-dimensional effects (device scales perfectly with its width).
- Neglect impact of substrate that surrounds the transistor

Definitions of spacial coordinates and voltages:



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Key conclusions

- *Deep depletion*: condition of MOS structure suddently switched from below threshold to above threshold.
- Application of voltage to inversion layer with respect to substrate shifts threshold voltage: $V_{SB} \uparrow \Rightarrow V_{th} \uparrow$.

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