Lecture 19 - Metal-Semiconductor Junction
(cont.)

March 19, 2007

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1. Schottky diode
2. Ohmic contact

Reading assignment:

del Alamo, Ch. 7, §§7.3-7.5

Key questions

- What is the basic structure of a Schottky diode? What are its most important parasitics?
- What are key technological constraints in the design and fabrication of Schottky diodes?
- How are Schottky diodes modeled for circuit design?
- How do Schottky diodes switch? What sets their time response?
- What does one have to do for a metal-semiconductor junction to become an ohmic contact?
- Why do ohmic contacts look as $S = \infty$ for minority carriers?

1. Schottky diode

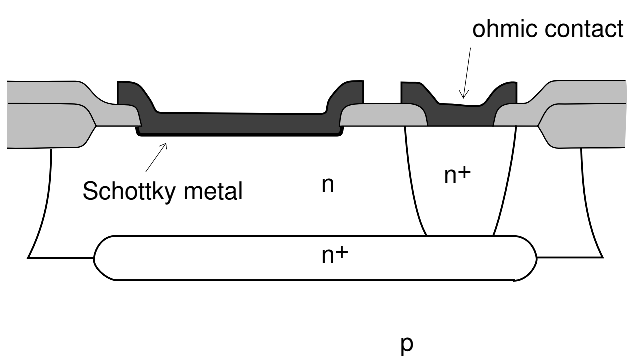
Key uniqueness: fast switching from ON to OFF and back.

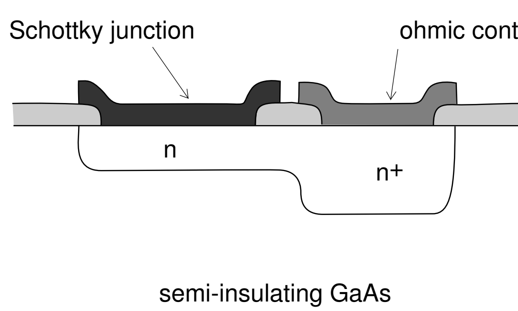
Widely used:

- in analog circuits: in track and hold circuits in A/D converters, pin drivers of IC test equipment
- in communications and radar applications: as detectors and mixers, also as varactors

Technological constraint: Schottky diodes engineered using process modules developed for other circuit elements → demands resourcefulness and imagination from device designer.

Typical implementations:



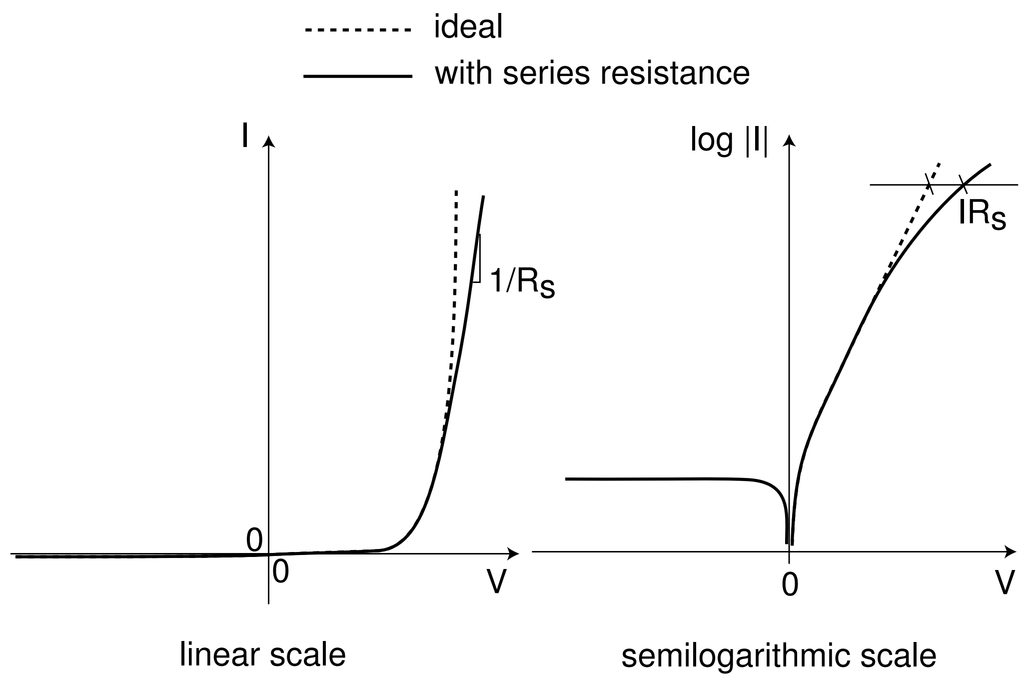


Parasitics

□ *Series resistance* due to QNR ohmic drop

Voltage across junction is reduced and I-V characteristics modified:

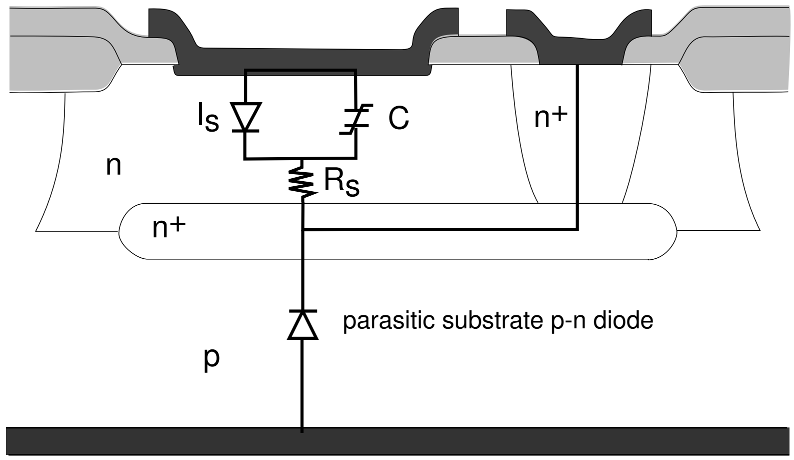
$$I = I_S[\exp\frac{q(V - IR_s)}{kT} - 1]$$



R_s bad because:

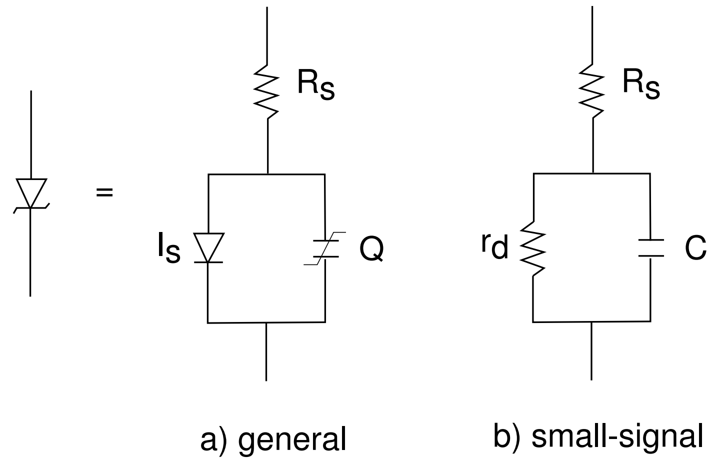
- for given forward current, V increased and harder to control
- it degrades dynamic response of diode

□ *Substrate capacitance*



Also degrades dynamics of diode.

Equivalent circuit models



□ *General model*:

"Ideal diode" in parallel with capacitor and in series with resistor.

Ideal diode is element with exponential I-V characteristics

$$I = I_S(\exp\frac{qV}{kT} - 1)$$

and no capacitance.

□ *Small-signal model*:

In many analog and communications circuits, Schottky diode is biased in some way and then a "small signal" is applied on top of bias → interested in response to small signal

Linearize general model:

$$\begin{aligned} I + i &= I_S \left[\exp \frac{q(V+v)}{kT} - 1\right] \\ &\simeq I_S \left[\exp \frac{qV}{kT}\left(1 + \frac{qv}{kT}\right) - 1\right] = I + \frac{q(I+I_S)}{kT} v \end{aligned}$$

For small signal, diode looks like resistor of *dynamic resistance*:

$$r_d = \frac{kT}{q(I+I_S)}$$

In forward bias, r_d only a function of I:

$$r_d \simeq \frac{kT}{qI}$$

In reverse bias, $r_d \to \infty$.

□ *Circuit CAD model* (such as SPICE)

In general, no specific Schottky diode model exists; p-n diode model is used.

Different models exist with different topologies. All of them described by **model parameters** (determined by device engineers).

Current in simplest model:

$$I_D = I_S A(\exp\frac{qV_j}{\mathbf{N}kT} - 1)$$

with:

$A \equiv$ relative area of modeled device and characterized device

and

$$I_S = \mathbf{IS}\left(\frac{T}{T_M}\right)^{\mathbf{XTI}} \exp[\frac{-q\mathbf{EG}}{k}(\frac{1}{T} - \frac{1}{T_M})]$$

Capacitance:

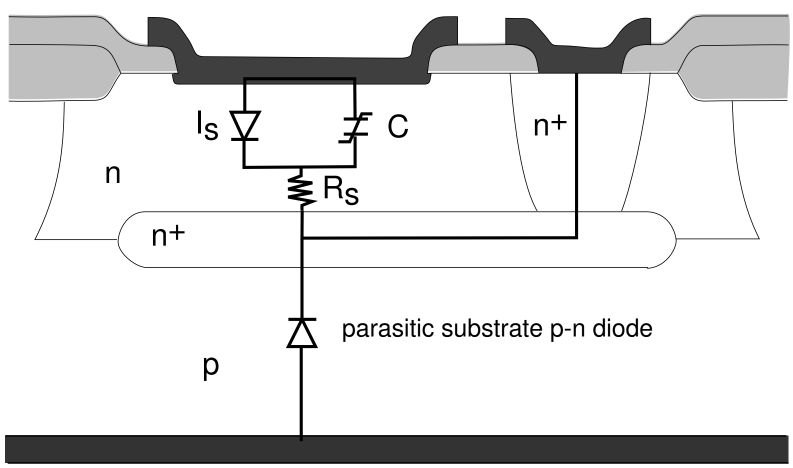
$$C = A\frac{\mathbf{CJO}}{(1 - \frac{V_j}{\mathbf{VJ}})^{\mathbf{M}}}$$

Additional models exist for breakdown, noise, additional leakage currents, other temperature effects, etc.

Summary of model parameters in simplest model:

name	parameter description	units	ideal value
IS	saturation current	A	-
N	ideality factor	-	1
EG	Schottky barrier height	V	-
RS	series resistance	Ω	-
CJO	zero bias depletion capacitance	F	-
VJ	built-in potential	V	-
M	grading coefficient	-	0.5
XTI	saturation current temperature exponent	-	2
TT	transit time	s	0
BV	breakdown voltage	V	-

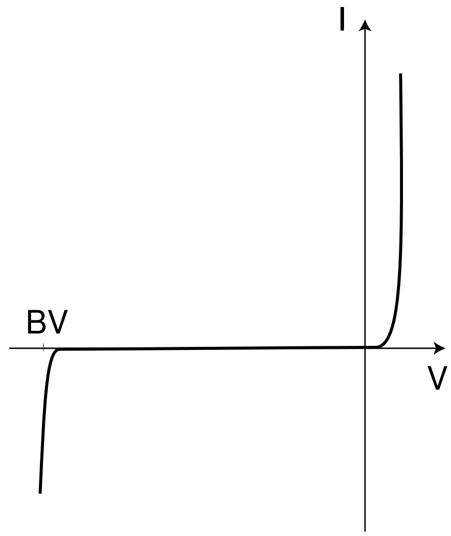
□ All models should account for parasitic substrate pn diode:

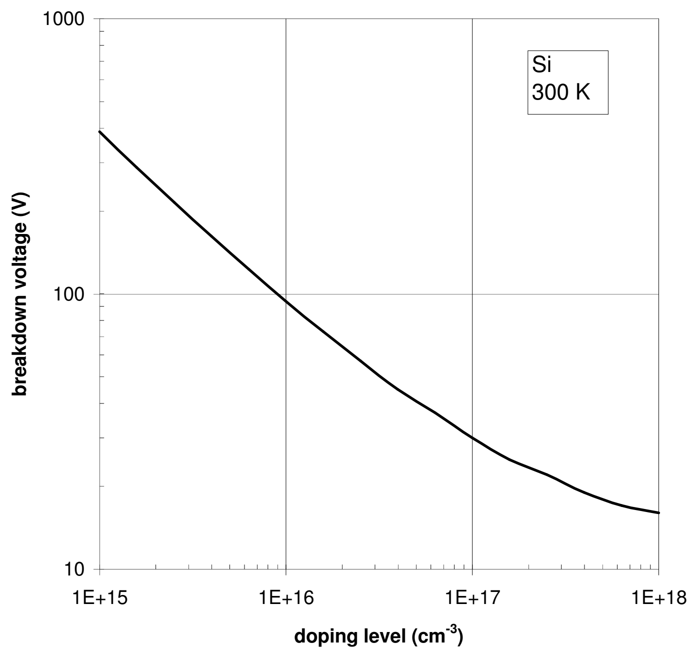


Breakdown

In reverse bias, as $|V| \uparrow \rightarrow |\mathcal{E}_{max}| \uparrow$

At a high-enough voltage, *avalanche breakdown* takes place → *breakdown voltage*





Computation of BV:

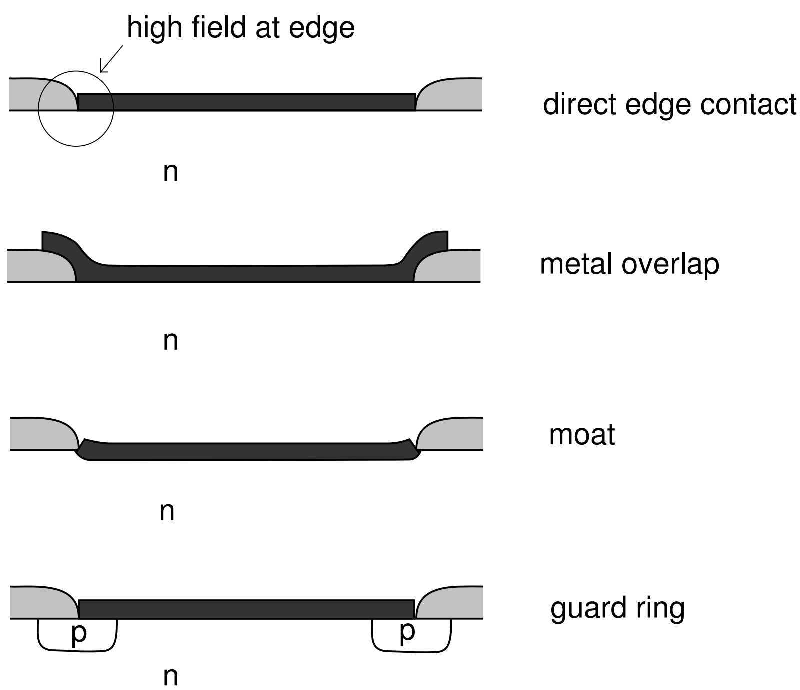
- Triggering current: I_S (all electron current for SBD on n-type semiconductor).
- Computation difficulty: $\mathcal{E}$ non-uniform in SCR.
- For moderate doping levels, BV function of N_D alone (independent of φ_{Bn}):

Technology, layout and design considerations

□ Often, no special metal is available → ohmic metal must be used

□ *Premature breakdown* may occur at edges of diodes.

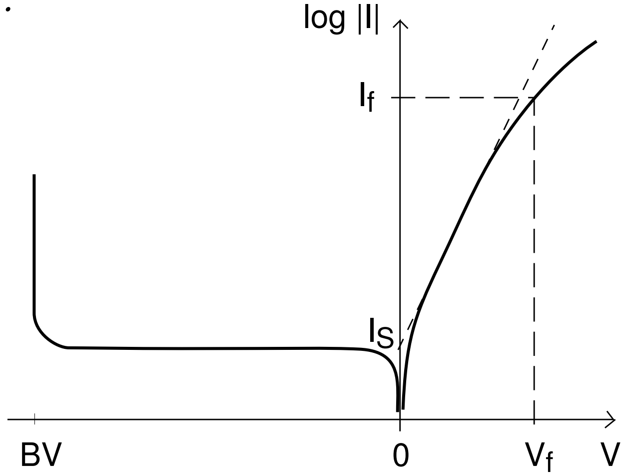
Premature breakdown mitigation requires "edge engineering":



If p guard ring used, must make sure that p-n junction never turns on.

In essence, this is a 2D or 3D problem.

□ *Design issues:*



- Metal selection:

$$\begin{aligned}\varphi_{Bn}\uparrow &\rightarrow V_f \text{ (for fixed } I_f) \uparrow\\ &\rightarrow I_S \downarrow\\ &\rightarrow \text{more } T \text{ sensitivity}\end{aligned}$$

- Doping level selection:

$$\begin{aligned}N_D\uparrow &\rightarrow R_s \downarrow\\ &\rightarrow C \uparrow\\ &\rightarrow BV \downarrow\end{aligned}$$

- Vertical extension of QNR:

  minimum value of t required to deliver BV (beyond that, $R_s \uparrow$)

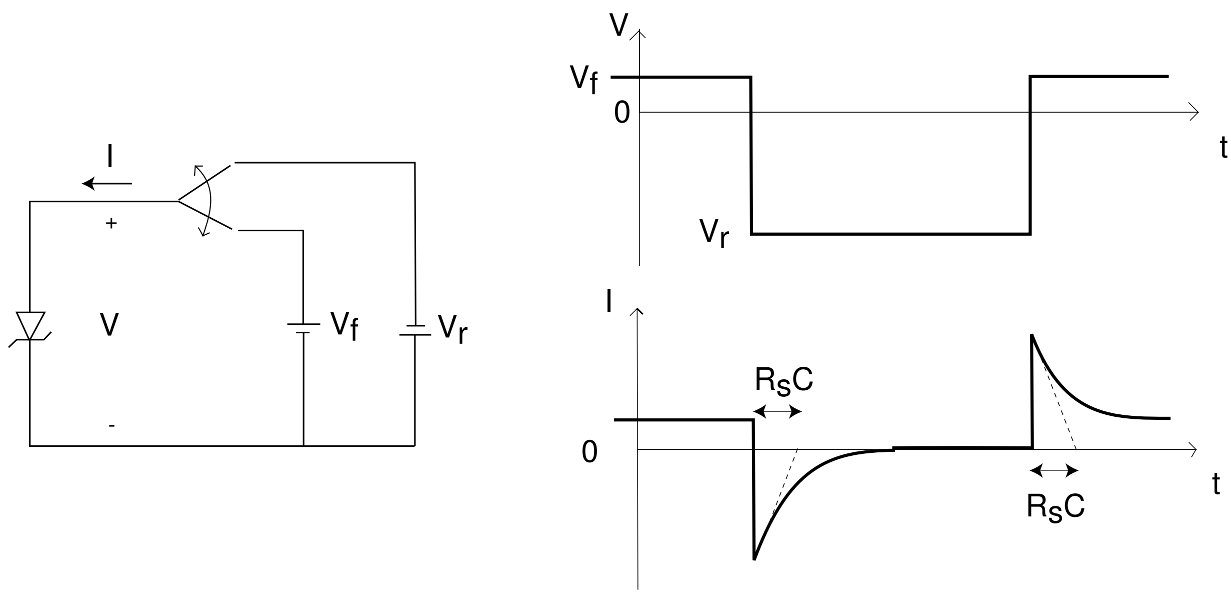
- Diode area:

$$\begin{aligned}A_j\uparrow &\rightarrow C \uparrow\\ &\rightarrow I_S \uparrow\\ &\rightarrow R_s \downarrow\\ &\rightarrow V_f \text{ (for fixed } I_f) \downarrow\\ &\rightarrow \text{more expensive}\end{aligned}$$

Dynamics

Uniqueness of Schottky diodes: they switch *fast*!

□ Large-signal example:



-switch-off transient: C charges up through R_s

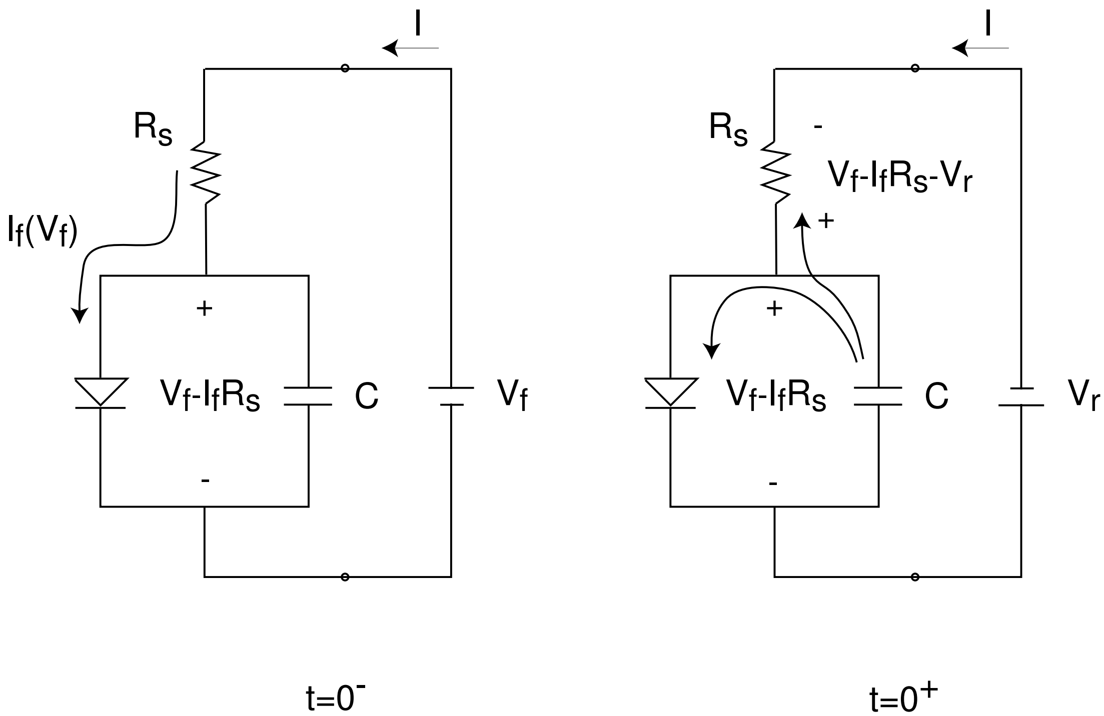
time constant: $\sim R_sC$

-switch-on transient: C discharges through R_s

time constant: $\sim R_sC$

for fast switching $\Rightarrow$ minimize R_s and C

Switch-off transient:

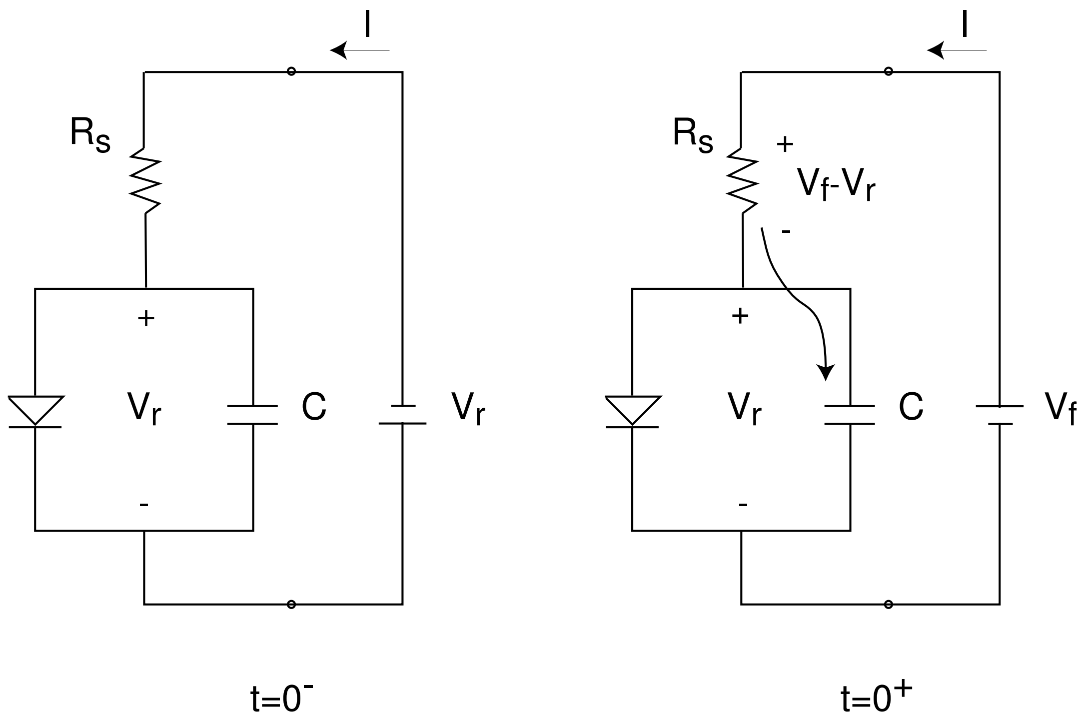


$$I(0^-) = I_f(V_f)$$

$$I(0^+) = -(\frac{V_f - V_r}{R_s} - I_f)$$

note: in this notation, V_r is negative

Switch-on transient:

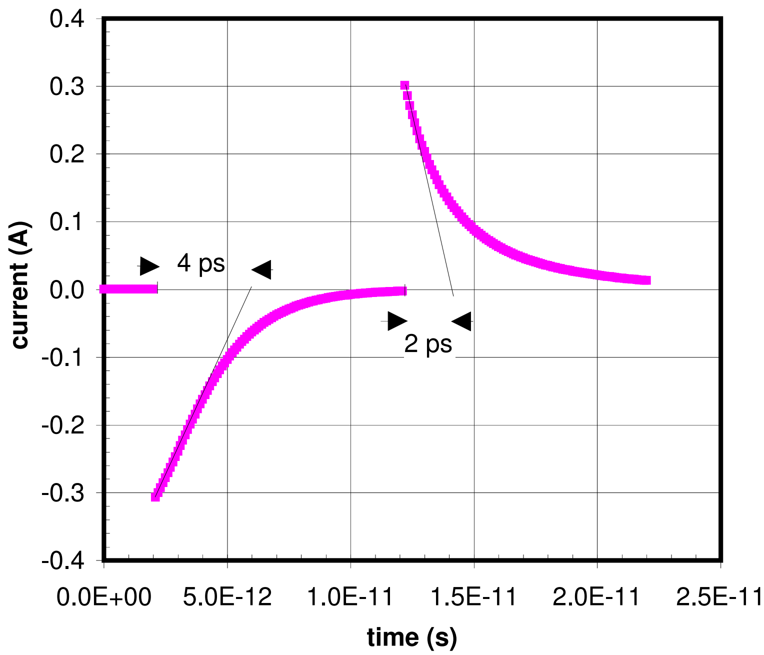


$$I(0^-) = -I_s \qquad\qquad I(0^+) = \frac{V_f - V_r}{R_s}$$

HSPICE example of large-signal switching:

SPICE Exercise: $V_f = 0.45\ V$, $V_r = 3\ V$.

Diode model parameters: **IS**$= 5.5e-13$, **N**$= 1.03$, **EG**$= 0.89$, **RS**$= 11$, **CJO**$= 3.24e-13$, **VJ**$= 0.5$, **M**$= 0.339$, **XTI**$= 2$, and **TT**$= 0$.



parameter	SPICE	hand calculation
τ_{off}	$4\ ps$	$7.8\ ps$
τ_{on}	$2\ ps$	$1.9\ ps$
$I_r(pk)$	$0.31\ A$	$0.31\ A$
$I_f(pk)$	$0.30\ A$	$0.31\ A$

2. Ohmic contact

• Ohmic contacts: means of electrical communication with outside world.

• Key requirement: very small resistance to carrier flow back and forth between metal and semiconductor.

• Ohmic contact = MS junction with large J_S

• V small $\rightarrow$ linearize I-V characteristics:

$$J \simeq A^*T^2 \exp\frac{-q\varphi_{Bn}}{kT}\frac{qV}{kT} = \frac{V}{\rho_c}$$

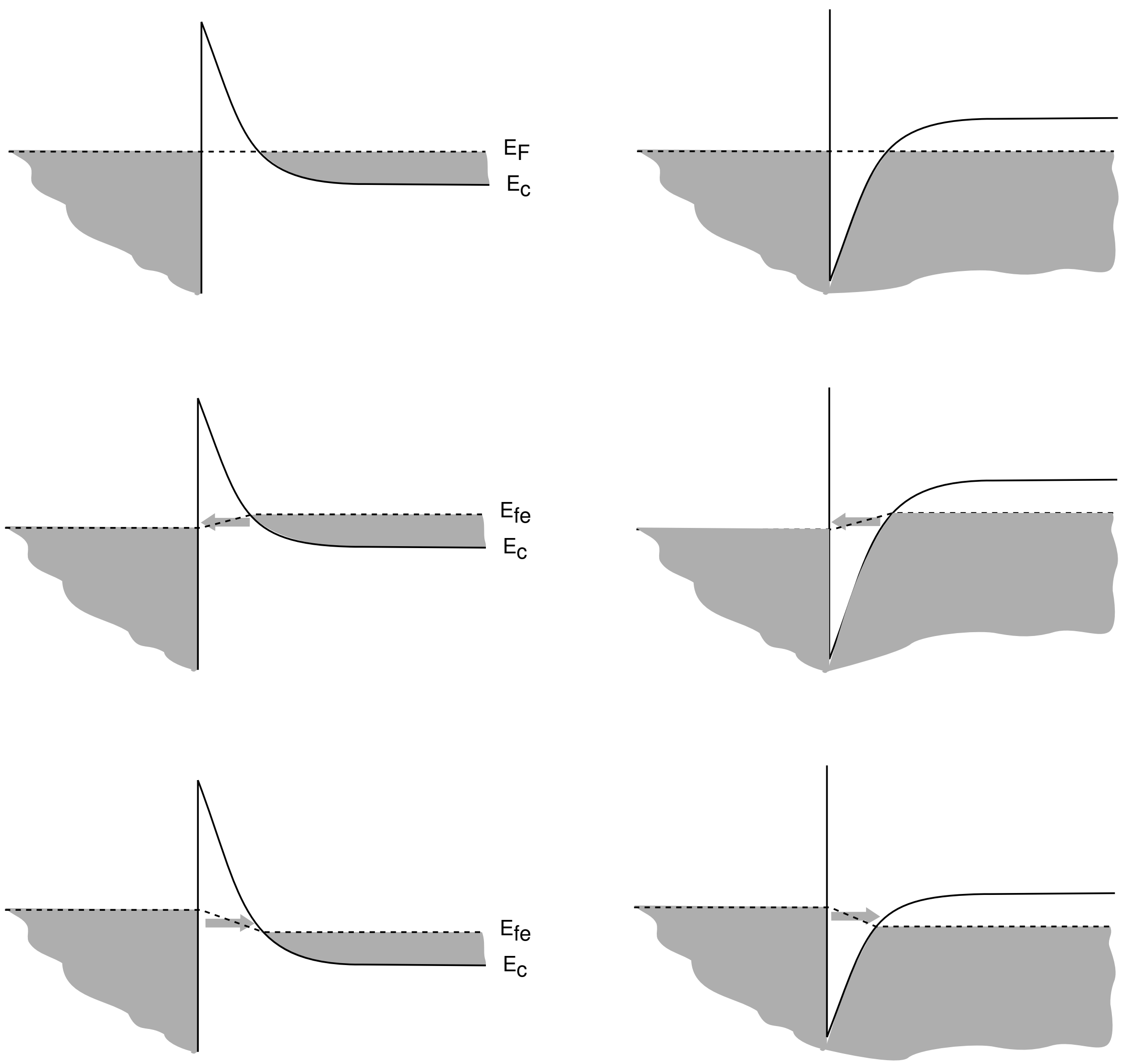
Figure of merit for ohmic contacts:

$$\rho_c \equiv \text{ohmic contact resistivity } (\Omega \cdot cm^2)$$

Good values: $\rho_c \leq 10^{-7}\ \Omega \cdot cm^2$

How does one make a good ohmic contact?

- Classically, use metal that yields small $q\varphi_{Bn}$
- Increase N_D until carrier *tunneling* is possible



ohmic contact to n-type semiconductor

ohmic contact to p-type semiconductor

Experimental measurements in n-Si:

Image removed due to copyright restrictions. Specific contact resistivity versus Nd graph.
Swirhun, Stanley Edward. "Characterization of Majority and Minority Carrier Transport in Heavily Doped Silicon." PhD diss., Stanford University, 1987. 340 pages.

Ohmic contact resistance:

$$R_c = \frac{\rho_c}{A_c}$$

$A_c \uparrow \Rightarrow \; R_c \downarrow$

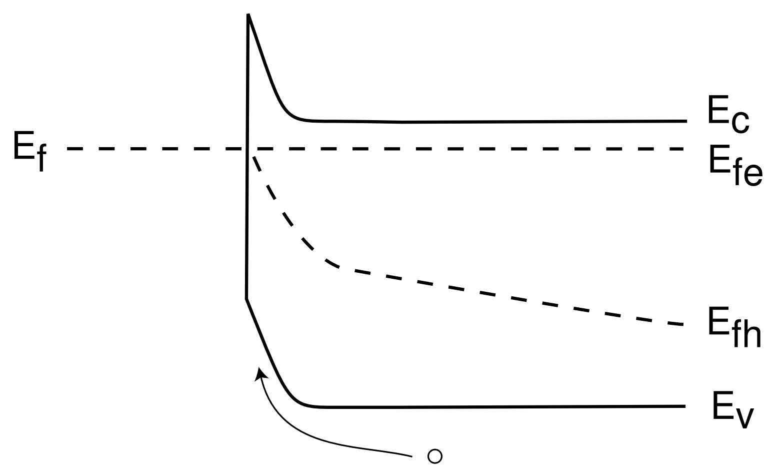
Justify two assumptions made earlier about ohmic contacts:

1) *Through a good ohmic contact, outside battery "grabs" majority carrier quasi-Fermi level.*

In "good" ohmic contact, R_c is very small $\Rightarrow V$ very small $\Rightarrow$ negligible difference in E_f across M-S interface.

2) $S = \infty$ *at ohmic contact*

Strong electric field at M-S interface "sucks" minority carriers towards it where they recombine:



In vicinity of ohmic contact, negligible concentration of excess minority carriers.

Key conclusions

- Main parasitics of Schottky diode: *series resistance* and *substrate capacitance*.
- Ideal BV of Schottky diode entirely set by doping level.
- Junction edge effects in Schottky diode may cause premature reverse breakdown.
- No minority carrier storage in Schottky diode $\Rightarrow$ fast switching.
- Dominant time constant of Schottky diode: R_sC.
- Typical design goals for Schottky diode: small time constant, high forward conduction, low reverse conduction, high breakdown voltage and small area. All without a dedicated process!
- Good ohmic contacts fabricated by increasing doping level $\Rightarrow$ carrier tunneling.
- ρ_c, *specific contact resistance* (in $\Omega{\cdot}cm^2$), proper figure of merit for ohmic contact.
- Order of magnitude of key parameters in Si at $300K$:
  - Desired specific contact resistance: $\rho_c < 10^{-7}\ \Omega \cdot cm^2$ (depends on metal and doping level).

Self study

- Small-signal dynamics of Schottky diode