# MASSACHUSETTS INSTITUTE OF TECHNOLOGY
### Department of Electrical Engineering and Computer Science

# 6.374: Analysis and Design of Digital Integrated Circuits
# Problem Set # 2

Fall 2003

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**For these problems you should use the parameters for the 0.25 technology (given in the text) unless otherwise specified for a particular problem.**

## Problem 1: Subthreshold Inverter Operation

In circuit applications where extremely low power consumption is essential and high speed operation is not required, subthreshold logic may provide an ideal solution. This problem will explore how far the supply voltage may be lowered before a CMOS inverter fails. For the entire problem, assume that the both devices are minimum length and that the NMOS device has a width of 0.44 um. Failure is defined as the point where an input swing of 0 to VDD produces an output swing less than 10% to 90% of VDD. For this problem use the 0.18 micron technology file which is located in "/mit/6.374/models/log018_1.l". (Research by Alice Wang)

a)  Consider the case where the input to the inverter is 0 V. Will the output voltage remain equal to the supply voltage as the supply voltage is lowered to arbitrarily low values? If not, explain what will happen and why. Would using a wider PMOS device increase or decrease the minimum possible supply voltage? Which process corner (TT, FF, SS, SF, or FS) will be the worst case and why? (Variable process conditions may result in a case where the NMOS and PMOS devices have modified mobilities. TT is the case where both devices are typical, SF has slow NMOS and fast PMOS, etc...)

b)  Consider the case where the input to the inverter is VDD. Would using a wider PMOS increase or decrease the minimum supply voltage in this case? Which process corner will be the worst case and why?

c)  Now, use HSPICE to simulate the inverter and find the lowest possible supply voltage. Complete one simulation for each input value using the process corners you chose in parts a and b. Use a .DATA statement to vary the width of the PMOS device across the set {0.5u, 1u, 1.5u, 2u, 4u, 8u, 10u, 15u, 30u, 45u, 60u} and sweep VDD from 100mV to 400 mV. Then, using the expressions function in AWaves, plot the ratio of V(out)/VDD. The points where the ratio crosses 0.1 and 0.9 are the failure points. Create a table with three columns containing: PMOS width, minimum supply voltage for the case where the input voltage equals 0, and minimum supply voltage for the case where the input voltage equals VDD.

d)  Now use your favorite graphing program (Matlab, Excel, etc....) to create a graphical representation for the functional region of operation. On a single graph, plot both cases of (minimum supply voltage, PMOS width) and indicate the region where both conditions are met. What is the lowest possible supply voltage that meets both conditions? What must the PMOS width be to operate at this supply voltage?

## Problem 2: CMOS Logic

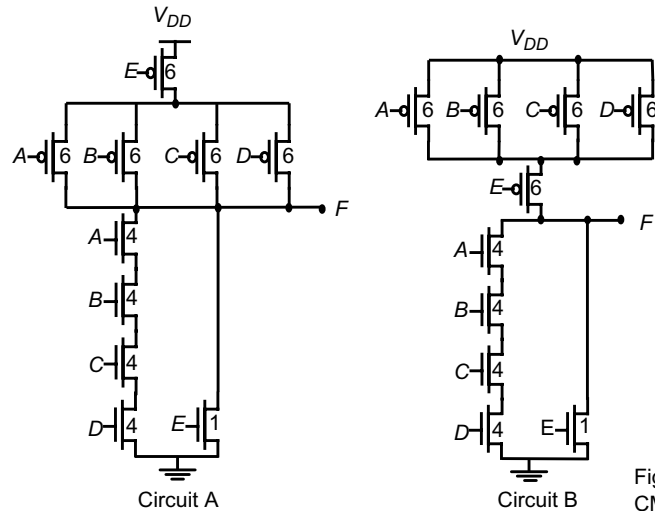Consider the following CMOS logic circuits:



Figure 0.1: Two static CMOS gates.

a) Do the two circuits in Figure 0.1 implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b) Assuming we can ignore all second order effects, do these two circuits have the same output resistances when driven with the same input patterns?

c) Assume the transistors have been sized to give a worst case output resistance of 13 kΩ for the worst-case input pattern. What input patterns ($A$–$E$) give the lowest output resistance when the output is low? What is the value of that resistance?

d) What input patterns ($A$–$E$) give the lowest output resistance when the output is high? What is the value of that resistance?

e) Neglecting parasitics and assuming a load capacitance of 100 fF, find the best case and worst case $t_{plh}$ and $t_{phl}$.

f) Now consider a few second order effects on the propagation delays. Which circuit is optimized for the case when it is known a priori that E will be the last input to arrive and why? How will body effect influence the performance of Circut A vs. Circut B?

g) For parts g and h, consider only Circuit B. Each intermediate node has some parasitic capacitance that must be charged and discharged at each transition. Therefore, the propagation delay is a function of both the initial voltage conditions on the internal nodes and the inputs. The inital voltage conditions, however, are determined by the previous inputs. Which set of previous and current inputs will cause the slowest $t_{plh}$? Which will cause the slowest $t_{phl}$?

h) Let all devices be minimum length and set the widths according to the relative scale in the diagram with 1=0.375 um, specify your source and drain areas and perimiters, and include an additional 10 fF load.

Use Nanosim to verify functionality by creating an input file which tests the following set of inputs [ABCDE]=[00000, 00001, 11110, 11100, 11111]. Verify that your simulated output values match the expected logic function. Submit your Nanosim output file.

## Problem 3: Pseudo-NMOS Logic

Consider the circuit of Figure 0.2.

a) What is the output voltage if only one input is high? If all four inputs are high?

b) What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

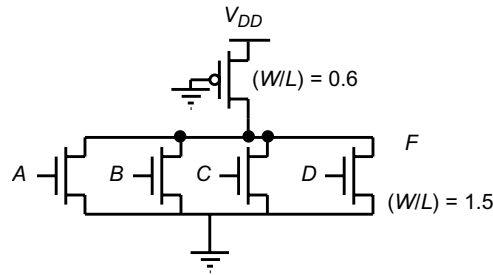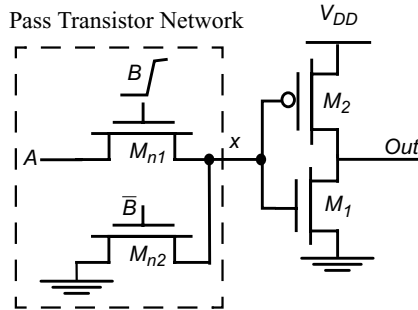c) Compare your analytically obtained results to a SPICE simulation.

Figure 0.2  Pseudo-NMOS gate.

## Problem 4: Pass Transistor Logic and Level Restoration

Consider the circuit of Figure 0.3. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

$V_{DD} = 2.5V$
$(W/L)_2 = 1.5um/0.25um$
$(W/L)_1 = 0.5um/0.25um$
$(W/L)_{ni} = 0.5um/0.25um$

$k_n' = 115uA/V^2$, $kp' = -30uA/V^2$
$V_{tN} = 0.43V$, $V_{tP} = -0.4V$

Figure 0.3  Level restoring circuit.

a) What is the logic function performed by this circuit?

b) Explain why this circuit has non-zero static dissipation.

c) Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d) Implement the same circuit using transmission gates.

e) Replace the pass-transistor network in Figure 0.3 with a pass transistor network that computes the following function: $x = ABC$ at the node x. Assume you have the true and complementary versions of the three inputs A,B and C.

## Problem 5: Device Modeling - DIBL

The standard equation for modeling subthreshold leakage current given in the notes is

$$I_d = I_o \cdot e^{\frac{V_{GS} - V_T}{nV_{th}}} \cdot \left( 1 - e^{\frac{-V_{DS}}{V_{th}}} \right).$$

This equation does not account for higher order effects like DIBL. The following BSIM equation adds the DIBL effect to the model:

$$I_d = I_o \cdot e^{\frac{V_{GS} - V_{To} - (\gamma' \cdot V_{SB}) + \eta \cdot V_{DS}}{nV_{th}}} \cdot \left( 1 - e^{\frac{-V_{DS}}{V_{th}}} \right).$$

Using this new equation, we will produce a model for the subthreshold leakage in the $0.25 \mu$ m process used in 6.374.

a) Using HSPICE, plot $I_d$ vs $V_{GS}$ for a single NMOS device with $V_D = V_{DD} = 2.5V$ and W/L = 0.5um/0.25um. We are only interested in the subthreshold region, so sweep $V_{GS}$ over the appropriate range.

Using HSPICE, plot $I_d$ vs $V_{DS}$ for $V_{GS}$=0V over the full range of $V_{DS}$. Plot the current on a log scale for both plots.

You will need to extract the points along these curves to use in your favorite analysis program (ie Matlab) for the rest of this problem. The following statement in HSPICE prints a table of the sweeping value and the current through a MOSFET to the HSPICE output stream: .print dc i(Mn1)

b) Using the data from the $I_o$ vs $V_{GS}$ plot, extract a value for S, the subthreshold slope, in mV/decade. Plot S as it varies with $V_{GS}$. Over which range of $V_{GS}$ is S likely to be the most accurate for modeling? Plot "instantaneous n" as it varies with S. Over which range is it likely to be accurate for modeling?

c) Now we will construct a model for the subthreshold behavior of the FET using the BSIM equation. This model should accurately represent the behavior of the FET that you saw in part a). The BSIM equation still is a reasonably low order model, so do not expect your final result to match the plots precisely - just try for a ballpark match. To develop the model, you need to select three parameters: $n$, $I_o$, and $\eta$ . The value for $n$ should be somewhere in the range that you plotted in b). Select $I_o$ so that the drain current supplied by the model matches the simulated value at $V_{GS}$=$V_{T0}$.

**Hints**: Pick an initial value for $\eta$ and use it with your estimates for $n$ and $I_o$ in the model equation for varying $V_{DS}$. $\eta$ controls the slope of the curve versus $V_{DS}$. Once the slopes are roughly equivalent, use your estimate of $\eta$ to find the current while sweeping $V_{GS}$. Select values of $n$ and $I_o$ that give a good fit. Now use those values in the other case to refine your choice of $\eta$ . Iterate this process a few times until you are satisfied with the models. It is helpful to convince yourself (by experimentation or from the equation) of the effects of the different param-

eters on the current. Remember, there is a range of "right" answers to this part of the problem. Also, be glad you don't do this for a living :)

Turn in a plot of $I_o$ vs $V_{GS}$ with the real data and the model data on the same plot. Do the same for $I_o$ vs $V_{DS}$. What were your values for $I_o$, $n$, and $\eta$ ? Comment **briefly** on what you consider to be a "good" fit using this model for this process (ie - is it more important to get the slope right or the actual values? is it better to overestimate or underestimate the current? etc). Why is your model a good choice?

## Problem 6: DCVSL Gate Design

a) Implement the function $S = ABC + A\overline{BC} + \overline{A}BC + \overline{A}B\overline{C}$ using transmission gate logic. What function does this circuit implement?

b) Now, design a DCVSL gate which implements the same function. Assume $A$, $B$, $C$, and their complements are available as inputs.

c) Simulate your DCVSL implementation in HSPICE with 30 fF load capacitance on each output. Assume that W/L = 0.5u/0.25u for all PMOS transistors and W/L = 2u/0.25u for all PMOS. Does your circuit work? If not, explain why and resize the PMOS devices to fix the problem.

d) Assuming $W/L = 0.5u/0.25u$ for *all nmos* transistors and $W/L = $ WP/0.25u for the *pmos* transistors (where WP is the value you chose in part c), produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1. Extract and simulate your circuit to verify functionality.