Problem Set #1: Updates and Frequently Asked Questions

Notes and Hints:

Problem 2:

- Some of you have asked about the regions of operation of the devices. Ignore the given VDD=2.5V and assume VDD is large enough that M1 does not go into subthreshold or linear operation when Vo is swept to 2.5 V. (You don't even need to know an exact value for this particular problem since lambda=0 - just assume it's large enough.) Given that condition, you know enough about VGT and VDSAT to determine the regions of operation.

Problem 3:

- Assume VDD=1.8 V for the entire problem. (To clarify, this does NOT mean that the drain is always connected to VDD! Think about the appropriate drain voltage for each section of the problem.)
- In part b, don't calculate entirely by hand. Use the I-V curves to find the resistance from the HSPICE simulation.
- For parts b and c you need only to consider the case where vdd=vgs(max)=1.8V. For parts a and d you may want to consider using .DATA and .MEASURE statements to make your work easier.

  The .DATA statement has syntax as follows and is used to repeat a particular transition for a set of conditions: (if you have parameterized vd in a statement .param vd=1.8v)

  .DATA D1 vd

  + 0.6

  + 0.8

  + 1.0

  + 1.2

  + 1.4

  + 1.6

  + 1.8

.ENDDATA

Then, in your transient analysis: .tran SWEEP DATA=D1 (Where step size and stop time are the values you have chosen. Given this parameterization, the easiest way to find and plot the propagation delays is to use .MEASURE statements. An example of this is: .MEASURE TRAN tdf TRIG V(in) VAL='vd/2' RISE=1 TARG V(out) VAL='vd/2' FALL=1 More documentation on how to use these statements is available in the complete documentation available through the course web page.

Problem 4:

- You will not get the same result for VOH by hand and with HSPICE. The hand calculation is based on the assumption that that M2 will stop charging the output node when the node reaches VDD-VT, (where VT includes body effect). In fact, transistors have non-zero subthreshold current and the final output voltage in the simulation is determined as several second order effects adjust the voltage to make the DC currents sum to zero. So, just use your VTC from part b to answer the questions in part c.

Problem 5:

- As stated, question 5a doesn't really make sense. Please reword 5a as follows: "The noise margins of a CMOS inverter are highly dependent on the sizing ratio, r=kp/kn, of the NMOS and PMOS transistors. What ratio 'r' would be required to achieve equal noise margins if the thresholds of NMOS and PMOS were equal and channel length modulation were ignored? Now use HSPICE and the 0.25u process file to test your theory. For your simulation, use Wn=1.0 um so that Wp will just be equal to r*(NMOS mobility/PMOS mobility). If there is a discrepancy in the two results you obtain, suggest some possible explanations."
- Some of you have asked about including vdsatp/vdsatn in the 'r' equation. For this problem only, do just use r as defined above for part a. You can think of this as the ideal case when threshold voltages, channel length modulation, and saturation voltages are equal for NMOS and PMOS. Since the vdsat terms are ratioed in this equation leaving out the two terms is equivalent to pretending they're equal. The explanation section is a good opportunity to discuss which of the prior assumptions might have been primarily responsible for causing any difference between your calculated 'r' in the above expression and the value you actually get from simulation.

Problem 6:

- For the parts of the problem involving Keq, find the C values for both transistions and average the results to get the effective capacitance.