MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.301 Solid State Circuits

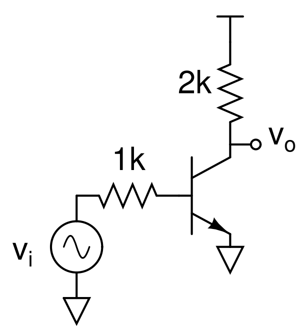
Fall Term 2010 | Issued : Sept. 24, 2010
Problem Set 4 | Due : Friday, Oct. 8, 2010

Suggested Reading: Read as many of the following as you can. All of the recommended references are on reserve at Barker Library.

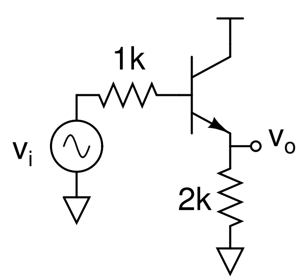
1. Lundberg sections 6, 7, 8, 9, and 10.
2. Grebene section 8.3-8.5.
3. Gray and Meyer sections 7.2 and 7.3.

Problem 1: The AC schematics for four amplifiers are shown below. For each of the amplifiers, find the midband voltage gain and the -3dB frequency using the open-circuit time-constant method. Assume β=200, I_C=2.5mA, c_π=50pF, and c_μ=2pF. Neglect r_b and r_o for this problem.

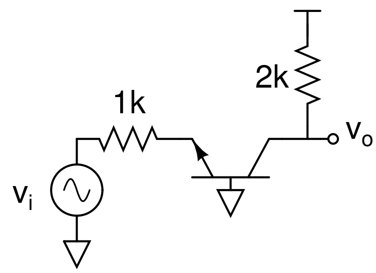
(a) Common-Emitter:



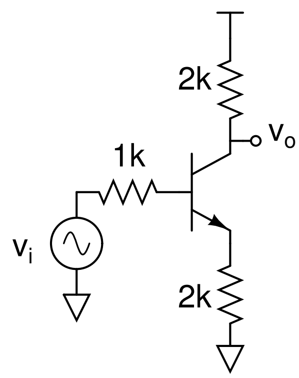
(b) Emitter-Follower:



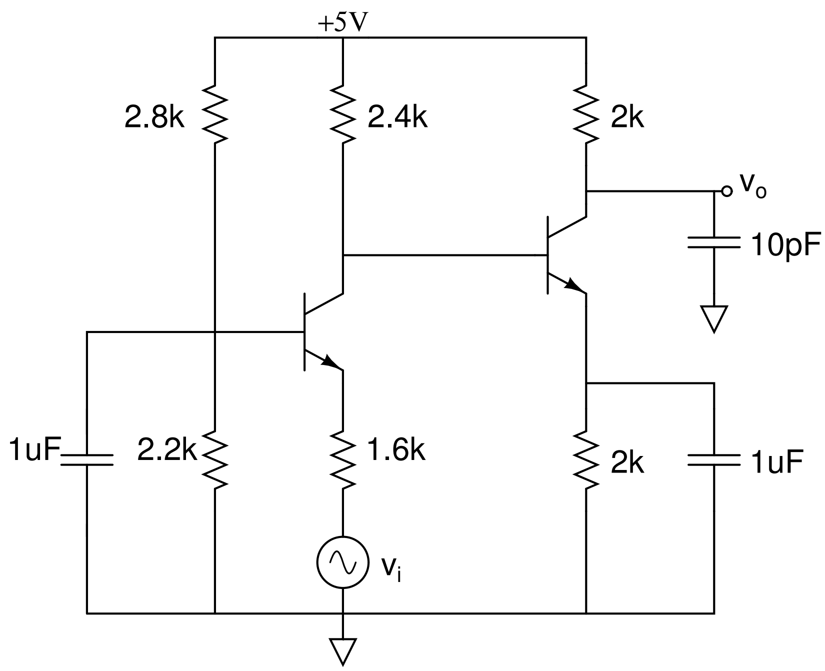
(c) Common-Base:



(d) CE with emitter degeneration:



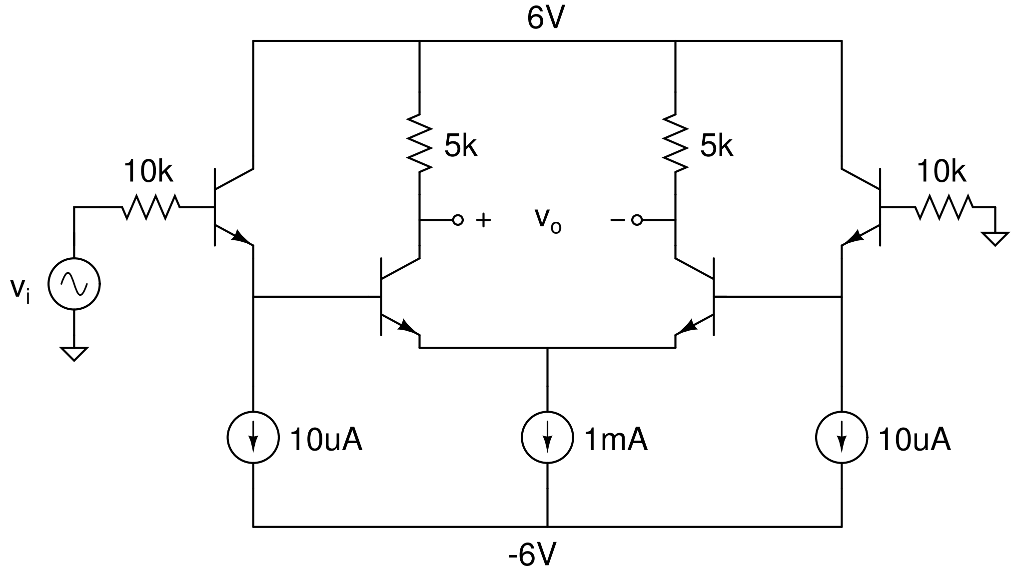
Problem 2: For the following CB-CE amplifier, assume that $V_{\text{BE,ON}}$=0.6V, β=200, c_π=20pF, and c_μ=2pF for both transistors. Neglect r_b and r_o.



(a) Calculate the midband small-signal voltage gain.

(b) Estimate the -3dB frequency of the circuit gain using the OCT method.

Problem 3: For the amplifer shown below, use the following data: I_S=0.5fA, β=200, $c_{\mu 0}$=0.5pF, c_{je}=4pF (in forward bias), and f_T=500MHz at I_C=1mA and V_{CB}=2.5V. Assume m=0.5 and Ψ_0=0.7V for all junctions. Neglect r_b and r_o.



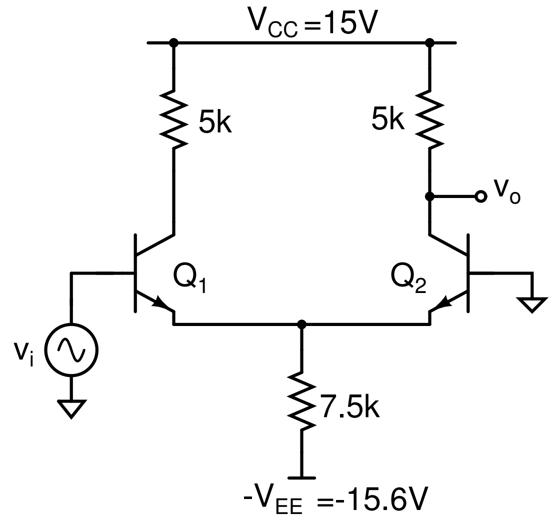
(a) Calculate the low-frequency voltage gain.

(b) Use the OCT method to calculate the -3dB frequency of the circuit gain.

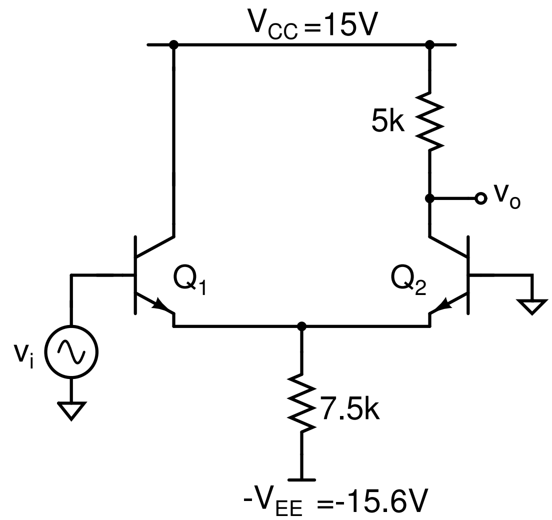
(c) Verify the above results in HSPICE. Turn in your HSPICE input file as well as a plot showing the high frequency roll-off.

Problem 4: For each of the two amplifiers shown below, assume that $V_{\mathrm{BE,ON}}$=0.6V, β=400, c_π=40pF, and c_μ=4pF for both transistors. You may neglect r_b and r_o. Find the small-signal voltage gain and the -3dB frequency. Qualitatively, why does one have more bandwidth than the other?

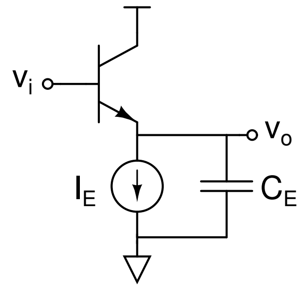
(a) Single-ended Differential Amplifier:



(b) EF-CB:



Problem 5: In recitation, a capacitively loaded EF such as the one shown below was discussed.



(a) Find the incremental input impedance. For simplicity, neglect c_μ in the small-signal model.

(b) Show that for sufficiently small values of C_E, the input impedance has a negative real part. Determine the critical value of C_E in terms of transistor parameters.

(c) Why could a negative input impedance be a bad thing?