Massachusetts Institute of Technology

Department of Electrical Engineering and Computer Science

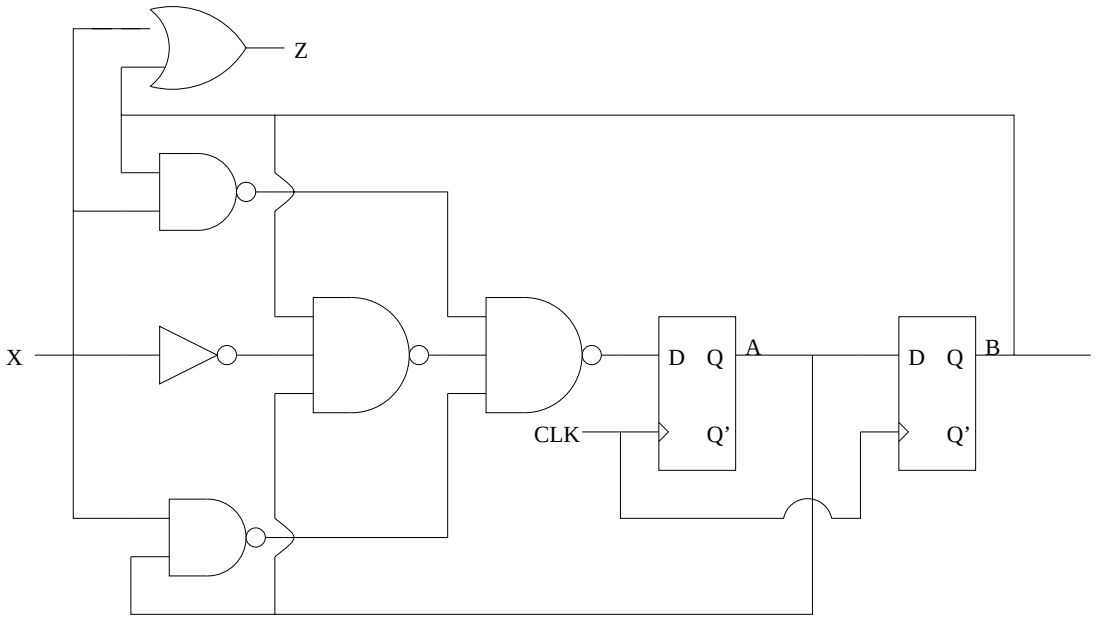
6.111 - Introductory Digital Systems Laboratory

Problem Set 3

Issued: Lecture 7 Day
Due: Lecture 10 Day

Problem 1:

A finite state machine shown below has one input, X, and one output, Z, and two state variables, A and B, and a clock input.

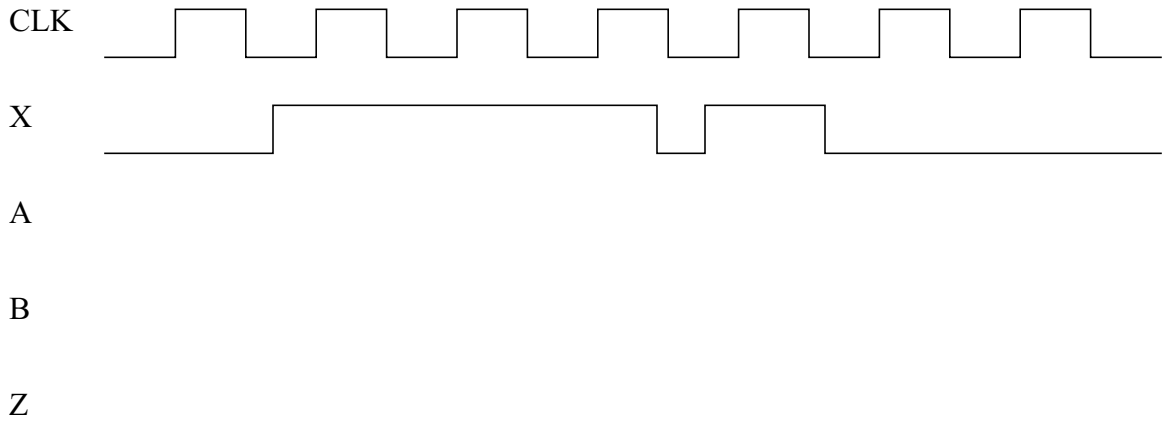


(a) Give the state transition table for this FSM.

(b) Draw the state diagram for this FSM.

(c) Implement this FSM in VHDL. Hand in your code and a printout of part of your simulation showing the correct operation of the FSM.

(d) Fill in the timing diagram below. You may neglect propagation delay in the logic, assuming it to be zero.



Problem 2:

Design a 3-bit counter that can count either up or down on the rising edge of the clock. There are three input signals: a clock signal, a reset signal, and a signal to indicate whether the counter should count up or count down. If the up/down signal is high, the counter will count up, if the input signal is low, the counter will count down. On reset, the count will return to zero.

(a) Give the state transition table for this FSM.

(b) Use K-maps to find the MSP expressions to be used as inputs to the D flip-flops.

(c) Draw the logic diagram for this counter.

Problem 3:

Using the minimum amount of logic, configure the LS163 4-bit counter to repeatedly count the following patterns:

(a) from 1 to 9 repeatedly, i.e. 1,2,3,4,5,6,7,8,9

(b) by even numbers, i.e. 0,2,4,6,8,10,12,14

(c) the sequence 0,2,3,6,9,10,15