DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE, MASSACHUSETTS 02139

Spring Term 2007
6.101 Introductory Analog Electronics Laboratory
Laboratory No. 3

READING ASSIGNMENT

In this laboratory, you will be investigating the performance of simple bipolar transistor and JFET amplifier circuits. Before doing this lab you should have read all of the reading assignments in the course outline through item 4 *Bipolar Transistors: transistor biasing;* and in item 5 *Field-Effect Transistors,* read the sections on *background* and *v-i characteristics;* and on *biasing*. Also read the class handouts on the hybrid-π equivalent circuit and transistor biasing. ***Note: Please read the whole lab before starting! You will be able to save time in those experiments where you have to repeat certain steps.***

Experiment 1: Transistor Biasing Schemes.

In this experiment you will compare two different transistor biasing schemes for DC "Q-point" stability. You will build the circuits of Figure 1a and 1b and measure the collector-to-ground voltage [V_{CG}] for each circuit using each of your four 2N3904 transistors. In all circuits, R_E = 1kΩ & R_L = 6.8 kΩ and the collector current should be 1.0 mA to give approximately 6.8 volts drop across R_L, a 1 volt drop across R_E, and about 7.2 volts drop across the collector-emitter junction of the transistor. [You will need the four 2N3904 transistors that you marked and for which you measured β_F in Laboratory 2. Be careful not to "fry" one of these devices, you will need them all!]

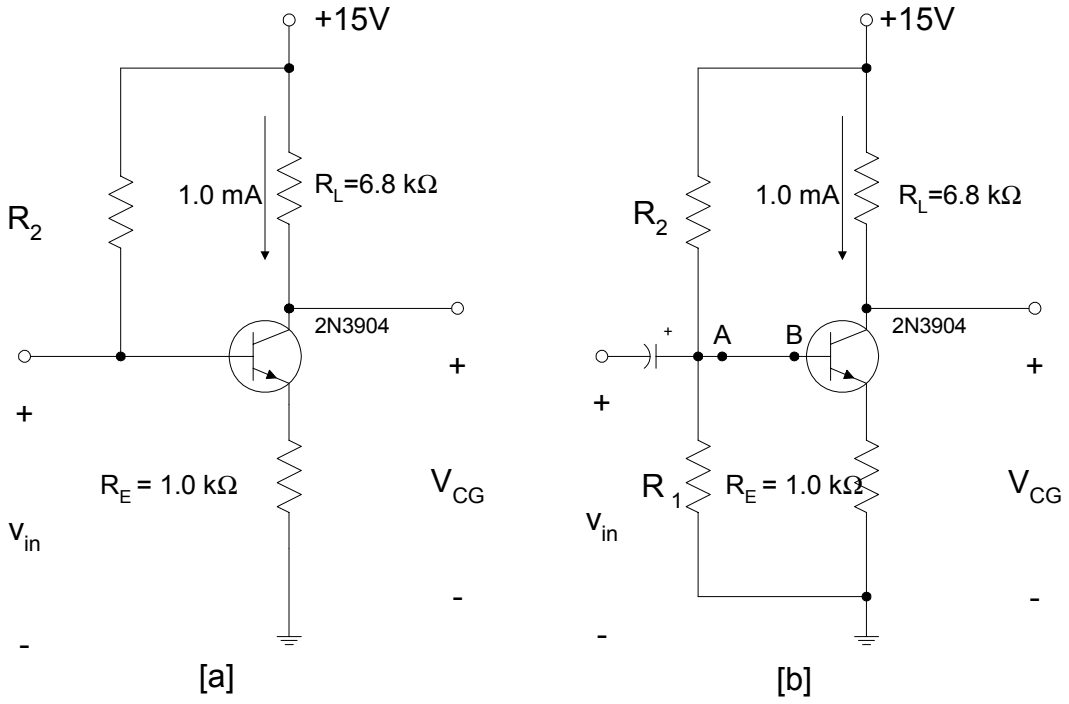
For each circuit, do the following:

1. Review the DC Beta [β_F] of your 2N3904's. For the best results in this experiment, your group of transistors should have a spread of β_F values of 1.5:1 or 2:1. If your devices do not exhibit this spread of values, please trade transistors with another 6.101 student; or trade in some of your devices at the drawers in building 38, on the 6th floor or at the stockroom window for different 2N3904's. You will have to measure the DC current gain on the curve tracer again if you take new devices, or you may use the M^3 Semiconductor Analyzer to select new devices. Note, however, that the M^3 measures the Beta at only the collector current value displayed.

2. Build the circuit of Figure 1a and calculate R_2 to provide the correct bias current for your 2N3904 that has the smallest value of β_F that you measured. The value of R_2 will probably be some odd value, not one of the standard resistor values available in your nerdkit or even not one of the 5% values from the drawers. Make up this odd value by putting standard values in series or in parallel until you achieve the nearest whole kilohm value to the value you calculated. Put your scope probe and DMM between collector and ground and measure V_{CG} ; it should be approximately 8.2 volts [7.2 volts across the C-E junction + 1 volt across R_E. Record your value for V_{CG} and then plug in the other three transistors, and record the value for V_{CG} that

each transistor gives. Turn the kit DC power switch to "off" when inserting and removing transistors. **Q 1.1 What would happen if you connected your scope probe from collector to emitter rather than collector to ground? Q 1.2 What would happen if you connected your DMM from collector to emitter rather than collector to ground? Q 1.3 Explain why V_{CG} varies so much from device to device.**

3. Now, you will repeat the above procedure for the circuit of Figure 1b. Using the same collector and emitter resistors, and I_C = 1.0 mA, and starting out with your transistor that has the lowest value of β_F, calculate the values of R_1 and R_2 using a Thevenin value for R_1 and R_2 of 10,000Ω. [This is the parallel combination of R_1 and R_2.] You should be able to come quite close to V_{CG} = +8.2 V using the two-resistor bias network. This time, you must use the closest standard +/- 5% values for R_1 and R_2. Repeat the process above by measuring the value of V_{CG} and recording it. Plug in transistor numbers 2-4 and again record the value for V_{CG} that each transistor gives.



Common Emitter Amplifiers
Figure 1: Transistor Biasing Circuits

Q 1.4 How do you explain the smaller differences in the value of V_{CG} that occur when you use the two-resistor circuit, compared to the single resistor circuit?

4. Draw the load line for the circuit of Figure 1b on the V_{CE} vs. I_C characteristics that you sketched for your transistor in Lab. No. 2. Clearly label the quiescent or operating point, as well as the base step currents.

Experiment 2: Transistor Amplifier AC Measurements

This experiment uses the circuit of Figure 1b above and the same resistor values that you calculated above. This circuit is known as a common-emitter amplifier and it is characterized by a voltage gain of $\frac{V_{out}}{V_{in}} = \frac{V_{cg}}{V_{in}} \approx A_v \approx \frac{-\beta_o R_L}{R_S + r_\pi + (\beta_o + 1)R_E}$, a high current gain, medium-to-low input impedance, and medium output impedance, usually equal to R_L. This gain equation holds as long as R_B [the parallel combination of the two biasing resistors] is large compared to R_S and r_π. However, when the emitter resistor is unbypassed, the second term in the denominator [$(\beta_o + 1)R_E$] is usually so large compared to the first two terms in the denominator, that the gain equation may be reduced to $A_v = -\frac{R_L}{R_E}$. Note that this equation is totally independent of transistor beta and transistor biasing [collector current], a very good situation since 5% resistors are far more stable in value from part-to-part than are transistor parameters!

1. Connect a 1 μF 15 Volt polarized electrolytic capacitor to the circuit as shown at point "A" with the + terminal of the cap toward the base and connect the negative lead of the capacitor to the output of your function generator [FG]. This capacitor is shown in Figure 1b. [**Q 2.1 Why should this capacitor be a polarized electrolytic instead of a non-polarized capacitor**? **Q 2.2 Under what conditions would you have to use a non-polarized capacitor in this application?**] Connect the function generator ground lead to your circuit ground. Make sure the DC offset voltage on your function generator is turned off. Break the connection between points "A" and "B" and insert a 1 kΩ 5% resistor between those two points. Adjust the generator's output voltage level until you measure a 3V-rms sine wave signal at 1000 Hz at the output of the amplifier [collector-to-ground]. The function generator output voltage is the amplifier input voltage, V_{in}. [The 1 kΩ resistor you have inserted is small compared to the input resistance of the *transistor* (**Q 2.3 What is the input resistance of this *transistor?***), so it has negligible effect on the circuit.]

The input impedance to this transistor is quite large, and can be calculated by using the hybrid-π equivalent circuit; but a quick approximation can be obtained from the product $\beta_o \times R_E$. However, in order to achieve bias stability, the value of R_B must be low compared to the AC input impedance, so with R_B shunting the AC input resistance, the actual input resistance to the *amplifier* is just R_B. [Please note the distinction between the input resistance to the **transistor** and the input resistance to the **amplifier**.]

Observe the output at the collector [$V_{cg} = V_{out}$] using your scope set on AC. If there is any "clipping" or distortion of the output signal, adjust the input level until the clipping stops.

2. Using your scope probes and/or your DMM set to AC, measure the input voltage and the output voltage, and calculate the voltage gain $A_v = v_{out} / v_{in}$. Repeat this measurement using all four transistors that you used in the DC measurements in experiment 1 above. **Q 2.4 How close do the voltage gains come to the approximation for voltage gain given above?**

3. In the common emitter configuration, in addition to a sizeable voltage gain, there is an AC current gain, β_o. The purpose of the 1 kΩ resistor you have inserted is to allow you to measure AC and DC base current. It may under some conditions be possible to insert a current meter to measure base current, but many of them have a high enough terminal impedance when set to measure low currents that they will change your DC operating point significantly. If you place

your DMM across the 1 kΩ resistor, you can read AC or DC current by setting the DMM to read AC or DC voltage. [25mV across the resistor will be equal to 25 μA of current.] Select one of your transistors for the circuit, and with the AC output voltage set as above, measure the AC current into the base. Calculate the AC current gain, β_o. Then, turn off your function generator's signal using the "output" button on the front panel . Measure the DC collector current by putting your DMM across R_L and also measure the DC base current. Calculate the DC current gain, β_F. Repeat this series of measurements for the other three transistors that you have characterized on the curve tracer.

Fill out the table below for the four transistors, and the values of DC and AC current gains that you obtained both from the experiment above and from the curve tracer. **Q 2.5 Do these values fall within the limits for these current gains that are given in the 2N3904 spec sheet?**
Q 2.6 How do the measured in-circuit β_F's compare %-wise with the β_F's you measured on the curve tracer? [This depends heavily on how carefully you set the "step zero" control on the curve tracer!]

4. Choose one device and install it in the circuit for Figure 1b. With a 1000 Hz signal at the input, adjust the magnitude of the input signal to produce some convenient output voltage value, say 1 Volt RMS, or 3 Volts peak-to-peak, depending on whether you want to measure with the DMM or the 'scope. Now, lower the frequency of the function generator until the output voltage has dropped to 0.707 of the value you noted at 1000 Hz. Record this frequency value.

5. Using the same device you used for step 4, replace the 1 μF capacitor with a 0.1 μF capacitor. Once again, choose a convenient output level at 1000 Hz, note it, and lower the input frequency until the output is again 0.707 of what it was, and record the frequency at which it happens. **Q 2.7 Why do you obtain different low frequency values for steps 4 and 5 above?**

6. Now, while observing the output waveform on the 'scope, remove the input coupling capacitor and replace it with a jumper wire. [You may do this with the power turned on if you are careful not to short adjacent wires.] **Q 2.8 What happens to the output signal when the capacitor is replaced by a wire jumper? Q 2.9 Explain why this happens in terms of the other circuit elements.**

Table for Transistor Gain Calculations

Circuit	2N3904 device #	Curve Tracer	AC volt. gain	AC curr. gain	DC volt. gain	DC curr. gain
DC Beta β_F h_{FE}	1		XXXXXXX	XXXXXXX		
	2		XXXXXXX	XXXXXXX		
	3		XXXXXXX	XXXXXXX		
	4		XXXXXXX	XXXXXXX		
AC Beta β_o	1				XXXXXXX	XXXXXXX
	2				XXXXXXX	XXXXXXX

h_{fe}	3				XXXXXXX	XXXXXXX
	4				XXXXXXX	XXXXXXX

Experiment 3: Bypassed emitter resistor voltage gain independent of β_o

If we place a large electrolytic capacitor across the emitter resistor, R_E, paying attention to polarity [positive capacitor terminal towards the emitter], the second term in the voltage gain equation above, [(β_o + 1)R_E] goes to zero, since for AC purposes, R_E is zero due to the capacitor bypassing it. This reduces our voltage gain equation from $A_v \approx \frac{-\beta_o R_L}{R_S + r_\pi + (\beta_o + 1)R_E}$ to $A_v \approx \frac{-\beta_o R_L}{R_S + r_\pi}$. Now, this equation shows a strong dependence on β_o, which is not good for gain stability from one circuit to another, when transistors of different betas are used. However, if R_s is small compared to r_π, then we can ignore the R_S term, and the equation looks like $A_v \approx \frac{-\beta_o R_L}{r_\pi}$. Since $\beta_o = g_m r_\pi$, the equation reduces to $A_v = -g_m R_L$. This shows that the voltage gain is only dependent on the transconductance, which equals $\mathbf{|I_C|/V_T}$, and the value of R_L. If we hold I_C steady thanks to our stable biasing scheme, then we have a voltage gain that is once again stable and only dependent on the value of R_L. Moreover, we are not limited to the relatively small values of gain obtainable with the unbypassed emitter resistance method $A_v = -\frac{R_L}{R_E}$; [the gain using this method is pretty much limited to values of –10 or less, unless you can live with very small output voltage swings or you use much larger supply voltages.] With the bypassed emitter method, $A_v = -g_m R_L$ easily yields gains of –200 to –300!

1. Install a 100 µF electrolytic capacitor across R_E paying attention to polarity. **Q 3.1 What is the minimum acceptable voltage rating for this capacitor? What would be a really wise choice for the voltage rating if you might change [accidentally or on purpose] the biasing conditions for this transistor?** Now, with the function generator connected, set the 1000 Hz output of the FG to a value that produces a nice 2 V p-p output signal that is not visibly distorted on the scope. Since the gain of this amplifier is quite high, you will probably need to use a voltage divider at the output of the function generator, as you did in Lab 1. A couple of 10 ohm resistors in parallel should work just fine and will lower the source impedance of the FG considerably, as well, helping to make our simplified gain equation even more accurate. Fill in the values in the following table, repeating all measurements for each of your four labeled transistors. You can probably leave the input voltage set to the same value for all transistors, as long as the output doesn't show any clipping or distortion.

Table for Transistor Gain Calculations, bypassed emitter resistor.

2N3904 device β_o	V_{CG} DC	V_{ac} input	V_{ac} output	Voltage gain	Calc. I_C	Calc. g_m	Calc. $-g_m R_L$	% error

Experiment 4: Field-effect Transistors.

In this experiment you will investigate the properties of a field effect transistor, specifically a 2N5459 junction field effect transistor [JFET]. This is an n-channel, depletion-mode device. It is controlled by a negative voltage applied between its gate and its source, with the drain-source current decreasing as the gate-source voltage gets more negative until the transistor is finally cut off and no drain-source current will flow.

1. Use the curve tracer to measure the drain-source [V_{DS} vs. I_D] characteristics of the 2N5459 JFET from your lab kit. Refer to the section entitled FIELD EFFECT TRANSISTORS on page 25 of the 577-177 manual. Don't forget that you must apply negative voltage steps to the gate of the JFET. Set the MAX PEAK POWER WATTS control back to 0.15 watts and the MAX PEAK VOLTAGE control to 25 volts. For the model 575, see p. 23 [attached] of the set-up charts. ***Be sure that you zero the V_{GS} = 0 curve using the switch that shorts the gate [base] to the source [emitter]. This switch is located at the bottom of the base step generator area of the 575. Be sure to ask for help if you don't understand how to do this.***

2. Measure the gate-source cutoff voltage $V_{GS[off]}$ which is different for every device [see 2N5459 characteristics handout]. This is the gate-source voltage for which no drain current flows. [The device is "off".] Also, measure I_{DSS}, the current that flows through the JFET when V_{GS} = 0. Your M^3 tester can verify your curve tracer measurements for these parameters.

3. From the output characteristics displayed on the curve tracer, make note of the area of those characteristics around I_D = 1 mA. [Your curves will be most useful if you try to get I_D = 1 mA about halfway up the curve tracer vertical [current] scale. You will need to know the value of V_{GS} in the vicinity of V_{DS} = 6-8 volts so that you can calculate the self-biasing resistor R_S for your amplifier. You may want to readjust the horizontal and vertical gain settings of your display so as to get these values near the middle of the scope display, as they will be more accurately read in the center of the display.

4. From the curve tracer display of the V_{DS} - I_D characteristics make a plot on linear graph paper in your lab notebook, or use the specially modified curve tracer to print the characteristics to a disc.

5. Construct the circuit of Figure 2. Use R_D = 6.2kΩ. Connect the scope probes to the V_{IN} and V_{OUT} terminals. Choose R_S to produce a static operating drain current I_D = 1 mA. Use the characteristic curves you drew in step 4 to help you choose the correct value of V_{GS} to produce this 1 mA drain current. Note that depletion-mode JFET's conduct their maximum I_D with zero volts on the gate (= I_{DSS}). [Actually, one can go slightly above V_{GS} =0 but the gate-source junction will be biased "on" at about 0.6 volts making the input look like a forward-biased diode, with its characteristically low input resistance and non-linear voltage-current relationship. FET's are almost always used for their low noise, high input resistance and low input current, so biasing the gate-source junction "on" is not recommended.]

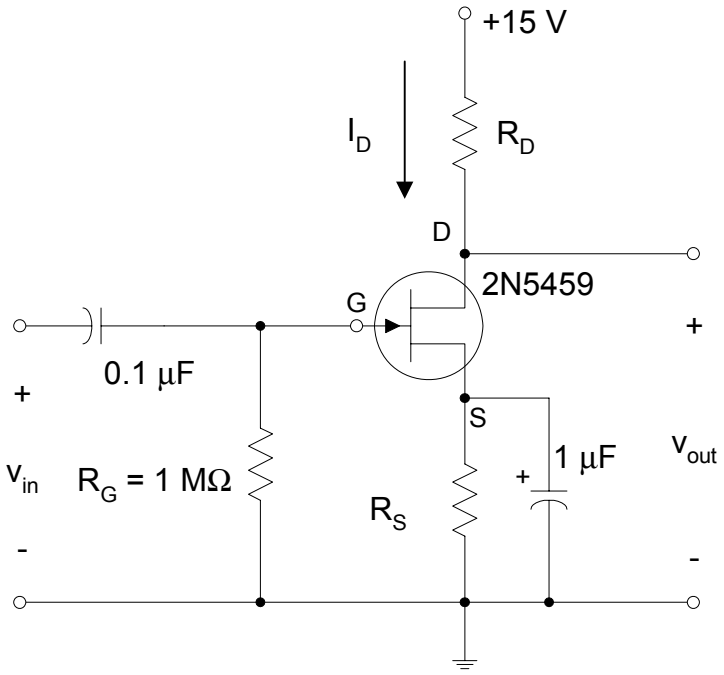


Figure 2: Circuit for Experiment 3.

6. With no signal input, measure the DC value of V_{OUT}. Subtract V_{RS} from $V_{OUT} = V_{DS}$ and locate the circuit Q-point [Quiescent or operating point] on the plot you made in step 4. Construct the output circuit load line using R_D, V_{DD}, etc. Ignore R_S.

7. Repeat item 6, but this time include the effect of R_S when you calculate the current axis intercept for the load line.

8. Based on the area of constant current output characteristics, mark the area of linear operation on the load lines you have constructed. Apply a 1000 Hz sine wave to the input and verify that you see a clean sine wave output at the peak-peak amplitude you marked on your load line. Increase the input voltage and observe the distortion as one-half of the sine wave is driven into the so-called "linear" region of the characteristics.

9. Calculate voltage gain assuming the input capacitor [C_1 = 0.1 μF] and source-resistor bypass capacitor [C_2 = 1.0 μF] behave as short circuits.

10. Measure both the input and output peak-to-peak voltages while the device is producing a clean sine-wave output. Calculate [from measurements] the circuit voltage gain. Remove C_2 and repeat. **Q 4.1 Explain any changes in gain that you measure. Hint: what is the purpose of C_2 in the circuit?**

11. Measure or calculate the AC input impedance of this amplifier. **Q 4.2 How does this compare with the input impedance of the transistor amplifier you made in the previous experiment?**

Experiment 5: Wind Your Own Inductor

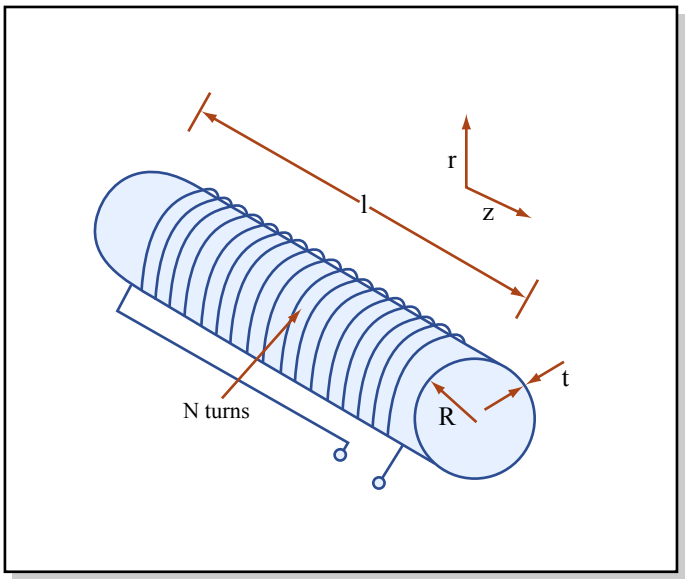


Figure by MIT Opencourseware.

Figure 3: Solenoidal Inductor

From elementary electromagnetic theory (for instance see Haus and Melcher, ***Electromagnetic Fields and Energy***) the inductance of a long, thin-walled solenoid is given by:

$$L \approx \frac{\mu_o N^2 \pi R^2}{l} \quad if \quad l >> R, t \qquad [1.]$$

This approximation is less valid for a thick winding [$t \approx l$] or a short, fat winding [$R \approx l$]. However, it's a useful order-of-magnitude estimate.

The series resistance of the winding is given by:

$$R_p = \frac{l_w}{\sigma_{Cu} a_w} \qquad [2.]$$

where l_w is the total length of wire used to wind the inductor, and a_w is the cross-sectional area of the wire.

Table 1: Important Physical Constants

μ_o, magnetic permeability of free space	$4\pi\times10^{-7}$ H/m
σ_{Cu}, electrical conductivity of copper	5.9×10^{7} $(\Omega\text{-m})^{-1}$

The electrical model makes sense; for very low frequencies, if you apply a voltage source the winding resistance (Rp) of the wire will limit the current. For high frequency, the current would be limited by the inductance of the solenoid. The parasitic capacitance C_p is due to the capacitance of each of the windings next to each other; for a practical inductor, the resonant frequency of the LC circuit will be much higher than your operating frequency, therefore the C_p can be ignored. It is important to note however, that this capacitance is real, and that if we drive the circuit from a voltage source through a large series resistor, we can observe resonance. This phenomenon is called ***self-resonance*** and is exhibited by all coils and capacitors.

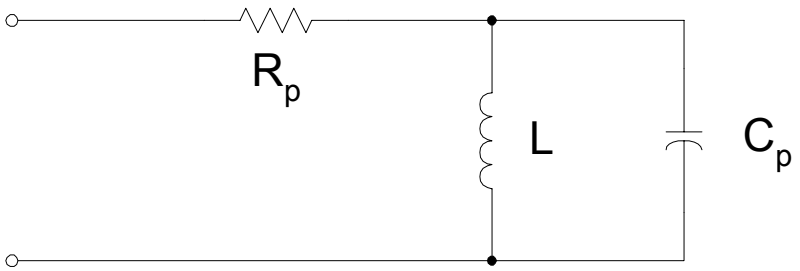


Figure 4: Electrical Model of Inductor

The impedance looking into the terminals of the inductor [ignoring C_p] is given by:

$$Z(j\omega) = R_p + j\omega L \qquad [3.]$$

1. Wind the inductor. Using #30 magnet wire (you can get this from the instrument desk, or from a spool in the 38-601 lab.), wind a closely-packed inductor with N=100 turns of magnet wire in a single layer on a pencil or other cylindrical winding form. The diameter of #30 gauge wire $\approx$ 0.01" = 2.54×10^{-4} meter. Make sure that the winding form isn't made of metal, or it will affect your L and R measurements! In order for the above approximation to hold, you want your solenoid to be much longer than its diameter, so don't use anything too thick as a winding form. Tape the wires down to the pencil so they won't move during your test. Measure the length and radius of your coil. Calculate the resulting inductance and lumped resistance. ***Note that magnet wire is insulated with a varnish or enamel coating. In order to use or measure your inductor, you will have to <u>scrape all of the enamel coating off the first inch of both ends of the wire.</u> Then you should solder short lengths of bare hookup wire to the fine magnet wires. Be sure you rotate the ends of the magnet wire as you scrape so that you will remove all the insulating coating. A penknife will work just fine.***

2. Measurements. Measure the value of L and R on the laboratory bridge, preferably the Hewlett-Packard 4192A Impedance Analyzer in building 38, on the 6th floor. There is another 4192A in lab on the 5th floor over in the 6.302 area, opposite room, and a complete instruction manual is chained to this 4192A. Use 1000 Hz as the measuring frequency; this will allow the bridge to resolve smaller values of inductance.

3. Test circuit. Build the circuit shown in Figure 5. Apply a 20 V p-p square wave at the input V_{in} and observe the output V_{out}. Adjust the frequency of the square wave over a wide range while observing V_{out}. **Q 5.1 Does this waveform make sense? Explain what's going on and put a sketch in your lab report. Make judicious use of engineering approximations!**

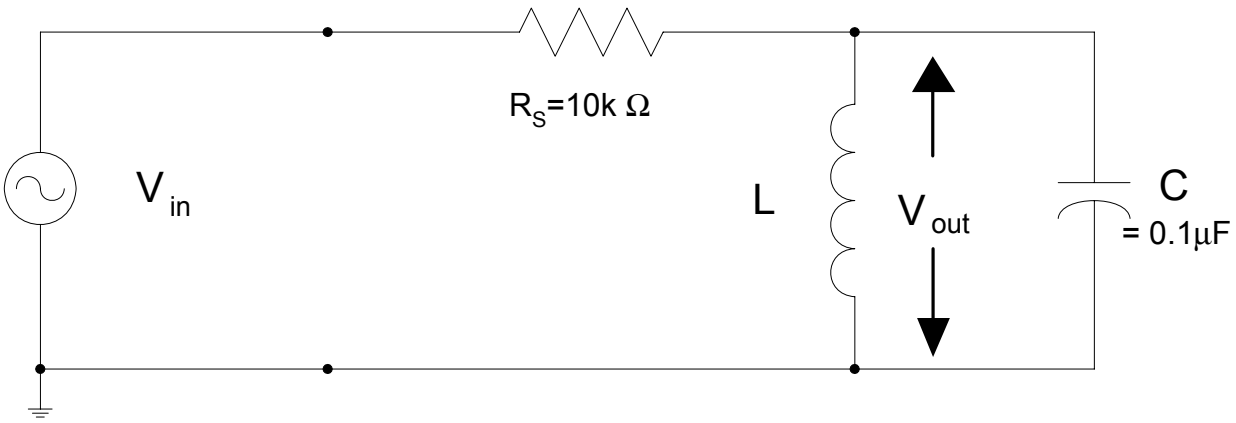
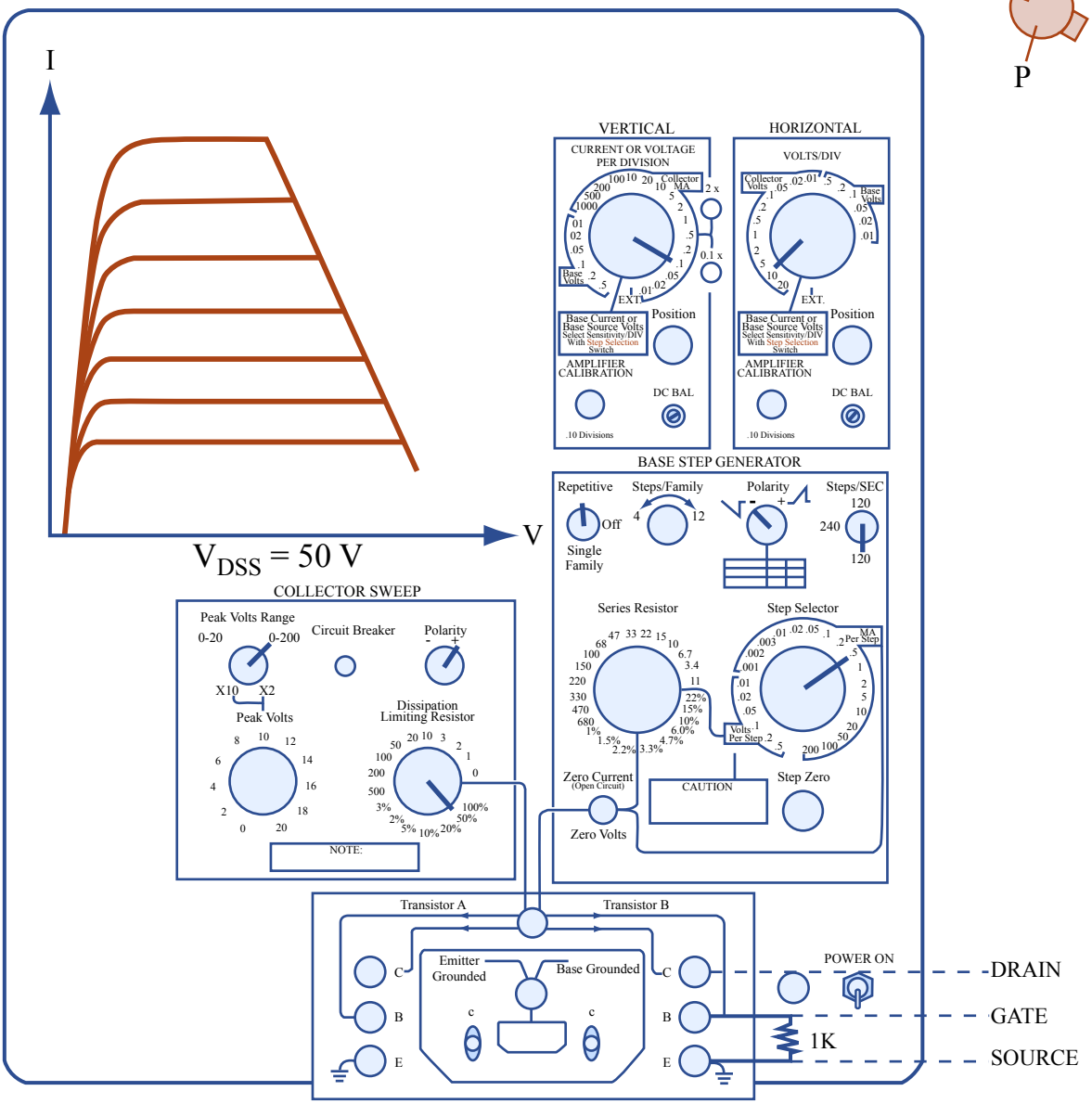


Figure 5: Circuit for Experiment 4

Note: R_s above is an external resistor. R_p in figure 4 is now "understood" to be a part of "L" in figure 5, and the C in figure 5 is an external capacitor, and C_p is also "understood" to be a part of "L" in figure 5.

Table 20.1 Copper Wire Data				
AWG SIZE	DIAMETER (MM)	Ω/KM (75°C)	KG/KM	TURNS/CM^2
0	8.250	0.392	475.00	
1	7.350	0.494	377.00	
2	6.540	0.624	299.00	
3	5.830	0.786	237.00	
4	5.190	0.991	188.00	
5	4.620	1.250	149.00	
6	4.120	1.580	118.00	
7	3.670	1.990	93.80	
8	3.260	2.510	74.40	
9	2.910	3.160	59.00	
10	2.590	3.990	46.80	14
11	2.310	5.030	37.10	17
12	2.050	6.340	29.40	22
13	1.830	7.990	23.30	27
14	1.630	10.100	18.50	34
15	1.450	12.700	14.70	40
16	1.290	16.000	11.60	51
17	1.150	20.200	9.23	63
18	1.020	25.500	7.32	79
19	0.912	32.100	5.80	98
20	0.812	40.500	4.60	123
21	0.723	51.100	3.65	153
22	0.644	64.400	2.89	192
23	0.573	81.200	2.30	237
24	0.511	102.000	1.82	293
25	0.455	129.000	1.44	364
26	0.405	163.000	1.15	454
27	0.361	205.000	1.10	575
28	0.321	259.000	1.39	710
29	0.286	327.000	1.75	871
30	0.255	412.000	2.21	1090
From Kassakian, Schlecht, Verghese: "Principles of Power Electronics"				

TYPE 575 TEST SET-UP CHART



DATA: F.E.T. 'N' CHANNEL

$$\text{TRANSCONDUCTANCE } (g_m) = \left.\frac{\Delta I_{DSS}}{\Delta Vgs}\right|_{V_{DSS}} = \left.\frac{160\mu A}{500mV}\right|_{V_{DSS}=50}$$

Non linearity is evident.

$$= 320\mu mhos$$

$$g_m(x) = g_m(0)\left[1-\left(\frac{V_{as}}{V_p}\right)^{2/3}\right]$$

$$A_V = g_m(x)R_L$$

Figure by MIT Opencourseware.