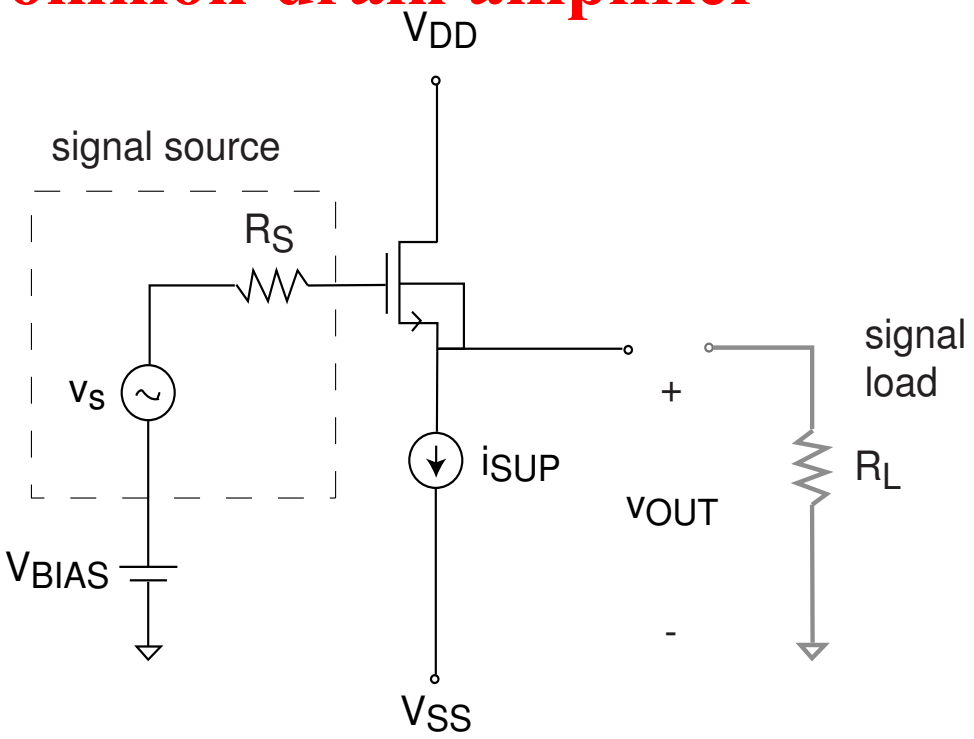
Lecture 20
Transistor Amplifiers (II)
Other Amplifier Stages

Outline

- Common-drain amplifier
- Common-gate amplifier

Reading Assignment:
Howe and Sodini; Chapter 8, Sections 8.7-8.9

1. Common-drain amplifier

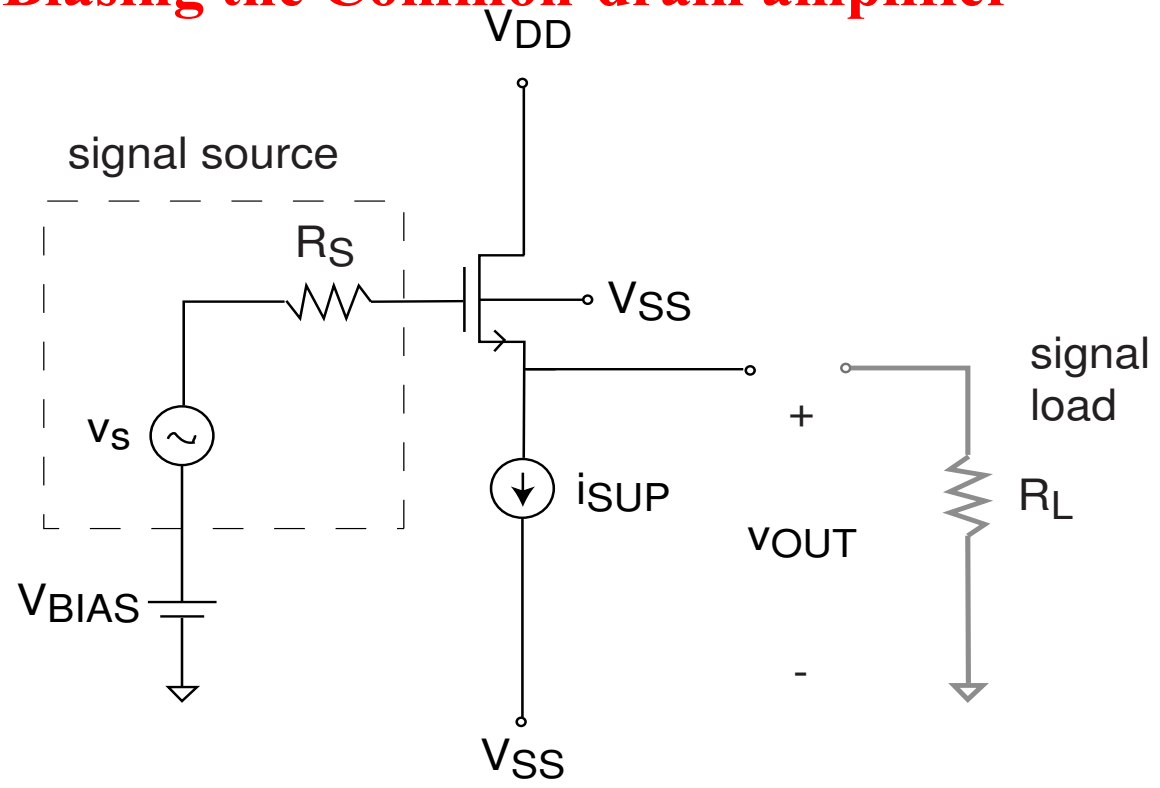


- A voltage buffer takes the input voltage which may have a relatively large Thevenin resistance and replicates the voltage at the output port, which has a low output resistance
- Input signal is applied to the gate
- Output is taken from the source
- To first order, voltage gain ≈ 1
- Input resistance is high
- Output resistance is low
  - Effective ***voltage buffer*** stage

How does it work?

- $v_{gate} \uparrow \Rightarrow i_D$ cannot change $\Rightarrow v_{source} \uparrow$
  - ***Source follower***

Biasing the Common-drain amplifier



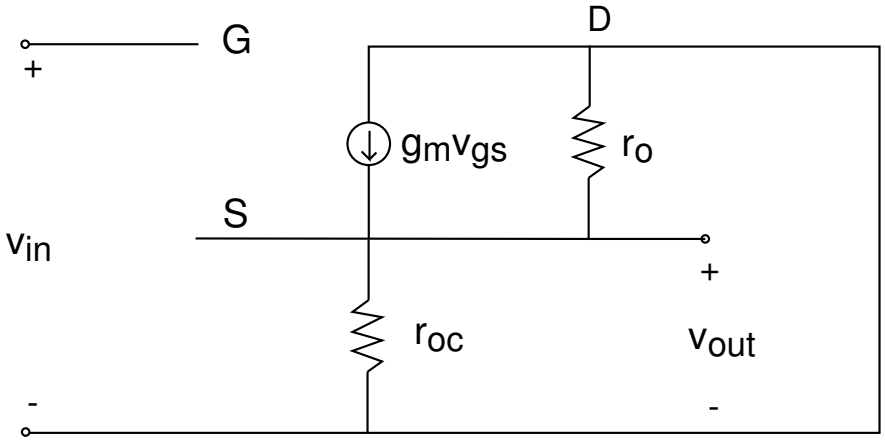
- Assume device in saturation; neglect R_S and R_L; neglect CLM ($\lambda = 0$)
- Obtain desired output bias voltage
  - Typically set V_{OUT} to"halfway" between V_{SS} and V_{DD}.
- Output voltage maximum V_{DD}-V_{DSsat}
- Output voltage minimum set by voltage requirement across I_{SUP}.

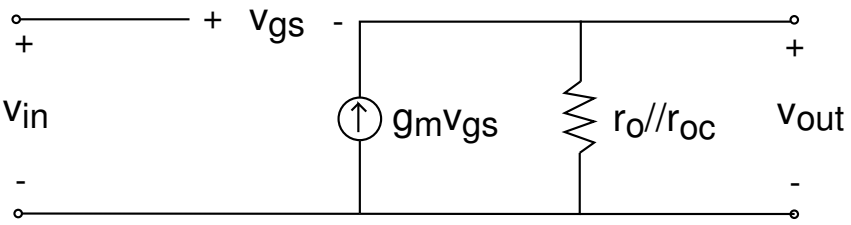
$$V_{BIAS} = V_{GS} + V_{OUT}$$

$$V_{GS} = V_{Tn}(V_{SB}) + \sqrt{\frac{I_{SUP}}{\frac{W}{2L}\mu_n C_{ox}}}$$

Small-signal Analysis

Unloaded small-signal equivalent circuit model:





$$v_{in} = v_{gs} + v_{out}$$

$$v_{out} = g_m v_{gs}(r_o \,//\, r_{oc})$$

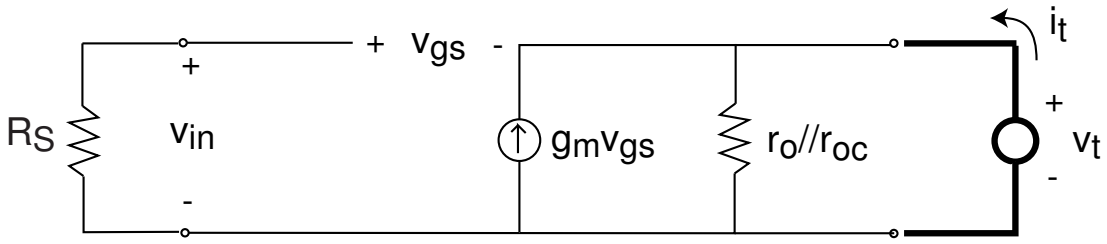
Then:

$$A_{vo} = \frac{g_m}{g_m + \dfrac{1}{r_o \,//\, r_{oc}}} \approx 1$$

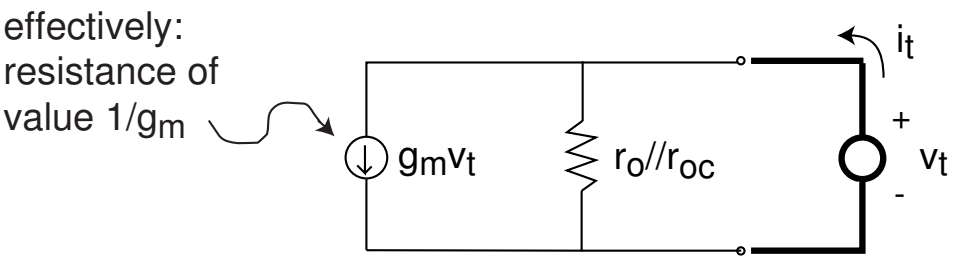
Input and Output Resistance

Input Impedance : $R_{in} = \infty$

Output Impedance:



$v_{in} = 0;\ v_t = -v_{gs}$



$$R_{out} = \frac{1}{g_m + \frac{1}{r_o // r_{oc}}} \approx \frac{1}{g_m}$$

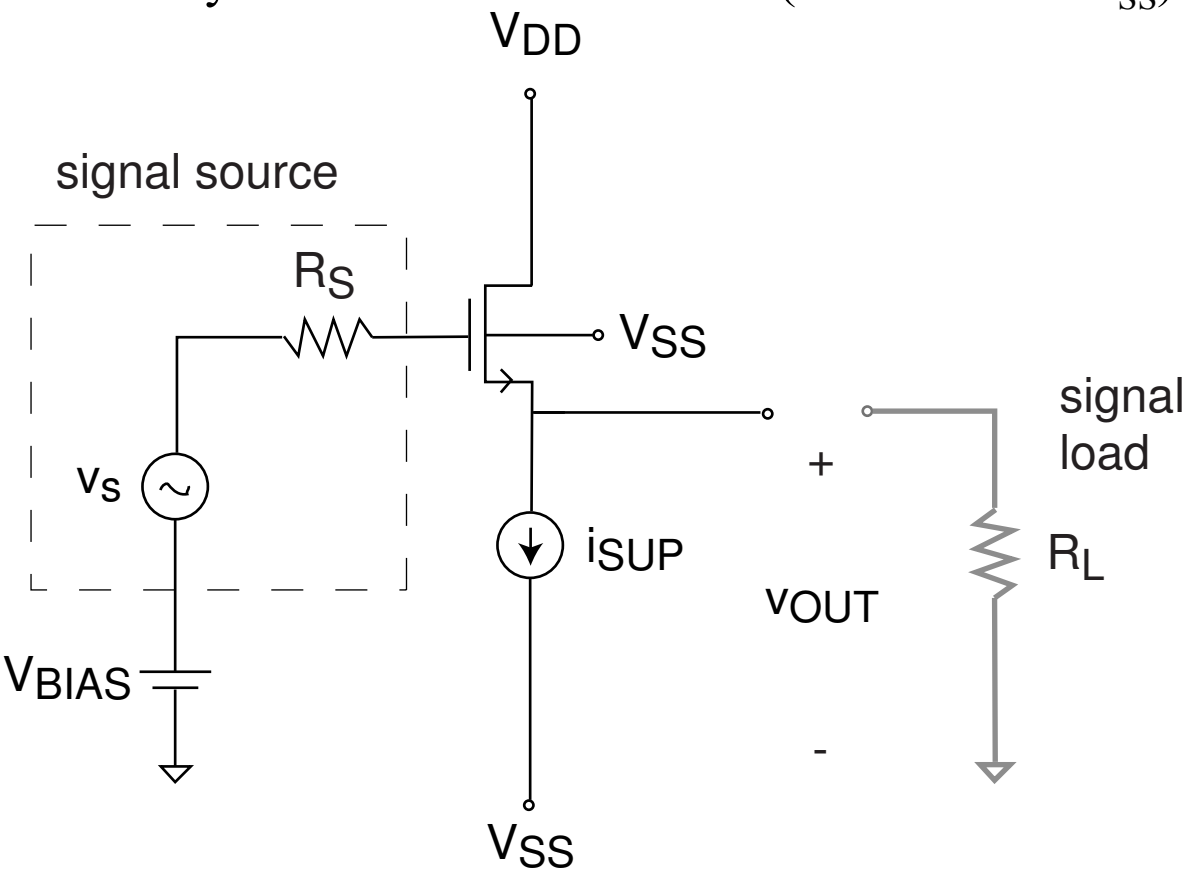
Small!

Loaded voltage gain:

$$A_v = A_{vo}\frac{R_L}{R_L + R_{out}} \approx \frac{R_L}{R_L + \frac{1}{g_m}} \approx 1$$

Effect of Back Bias

If MOSFET was not fabricated in an isolated p-well, then body is tied to wafer substrate (connected to V_{SS})

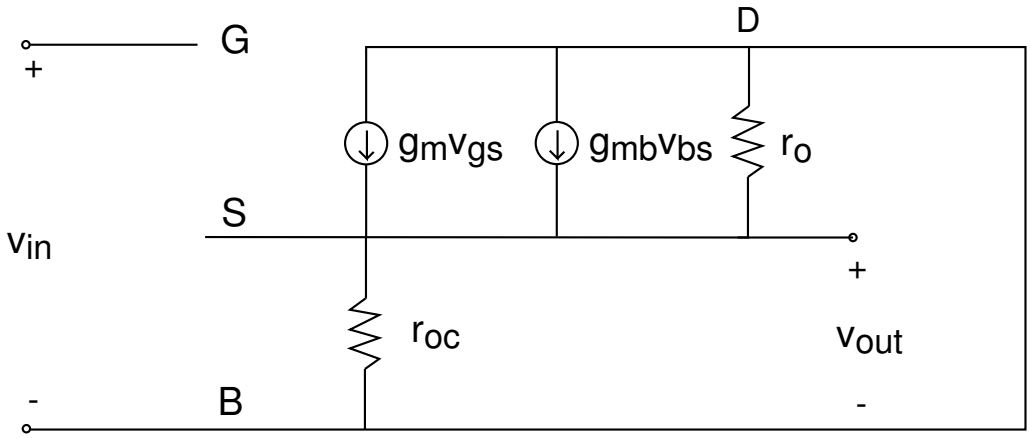


Two consequences:

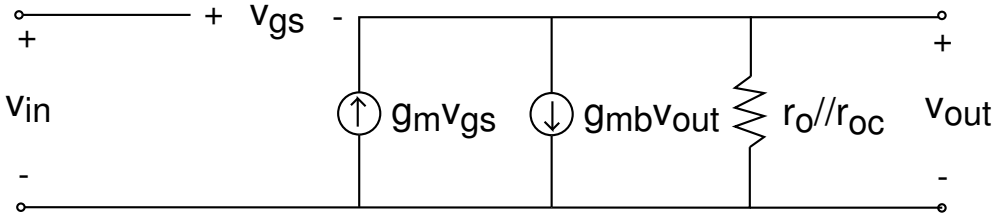
- Bias is affected
  - V_T depends on V_{BS}
  - $V_{BS} = V_{SS} - V_{OUT} \neq 0$
- Small signal figures of merit affected
  - Signal shows up between B and S
  - $v_{bs} = -v_{out}$

Small-signal Analysis (with back-bias)

See text pp.523-527 for details



vbs=-vout

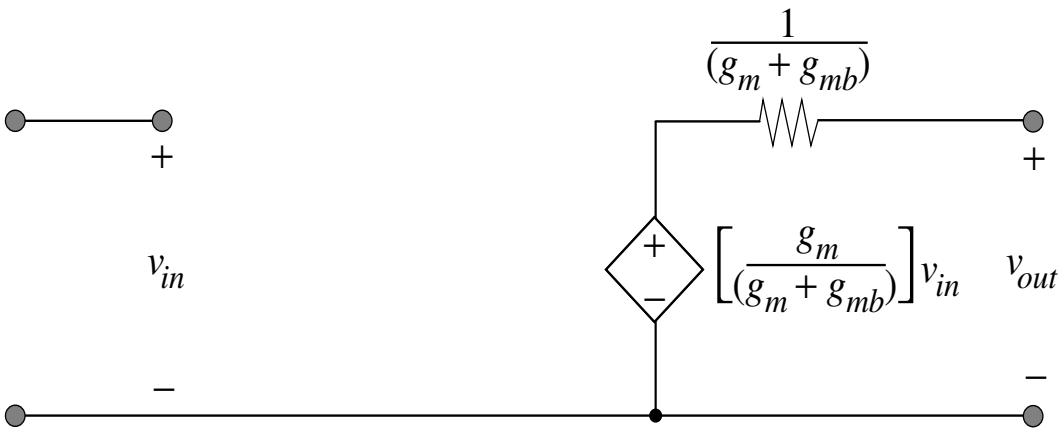


$$A_{vo} = \frac{g_m}{g_m + g_{mb} + \dfrac{1}{r_o \,//\, r_{oc}}} \approx \frac{g_m}{g_m + g_{mb}} < 1$$

Also:

$$R_{out} = \frac{1}{g_m + g_{mb} + \dfrac{1}{r_o \,//\, r_{oc}}} \approx \frac{1}{g_m + g_{mb}}$$

Common-Drain Two-Port Model



- Open circuit voltage gain ~ 1
- Input resistance ~ CS Amplifier
  - We want a large input resistance because the controlled generator is voltage controlled
- Output resistance << CS Amplifier
  - We want a low output resistance to deliver most of the output voltage to the load

Relationship between circuit parameters and device parameters:

$$g_m = \sqrt{2 I_D \frac{W}{L} \mu_n C_{ox}}$$

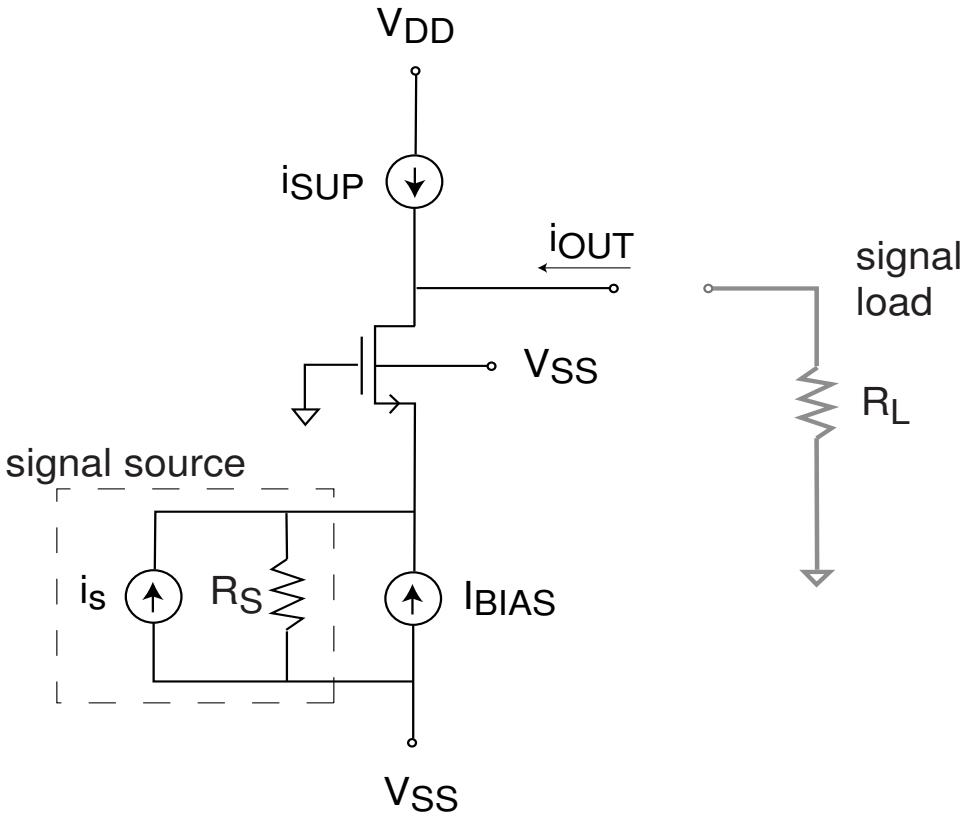
$$g_{mb} = \frac{\gamma}{2\sqrt{-2\phi_p - V_{BS}}} g_m$$

Device* Parameters	Circuit Parameters		
	$\lvert A_{vo} \rvert$	R_{in}	R_{out}
	$\frac{g_m}{g_m + g_{mb}}$	$\propto$	$\frac{1}{g_m + g_{mb}}$
$I_{SUP} \uparrow$	-	-	$\downarrow$
$W \uparrow$	-	-	$\downarrow$
$\mu_n C_{ox} \uparrow$	-	-	$\downarrow$
$L \uparrow$	-	-	$\uparrow$

* V_{BIAS} is adjusted so that none of the other parameters change

Common Drain amplifier is often used as a ***voltage buffer*** to drive small output loads (in multistage amplifiers, other stages provide the voltage gain).

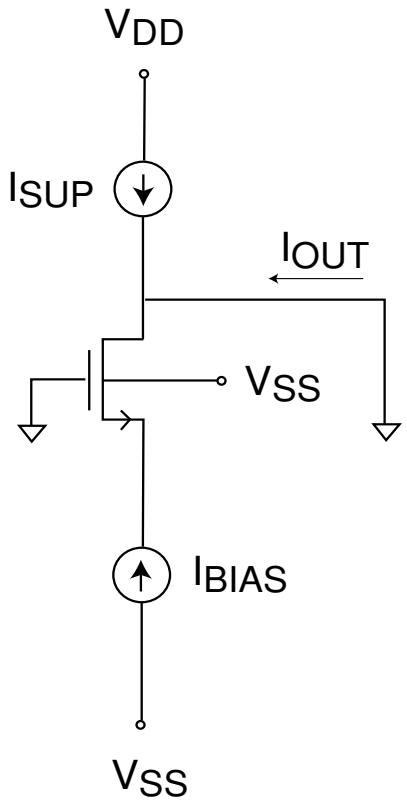
2. Common-Gate Amplifier:



- A current buffer takes the input current which may have a relatively small Norton resistance and replicates the current at the output port, which has a high output resistance
- Input signal is applied to the source
- Output is taken from the drain
- To first order, current gain ≈ 1
  - $i_s \approx -i_{out}$.(Current Buffer)
- Input resistance is low
- Output resistance is high
  - Effective ***current buffer*** stage

Biasing the Common-Gate Amplifier:

Assume device in saturation; neglect R_S and R_L; neglect CLM ($\lambda = 0$)



$$I_{SUP} + I_{OUT} + I_{BIAS} - 0$$

Select bias such that $I_{OUT}=0 \Rightarrow V_{OUT} = 0$.

Assume MOSFET in saturation (no channel modulation):

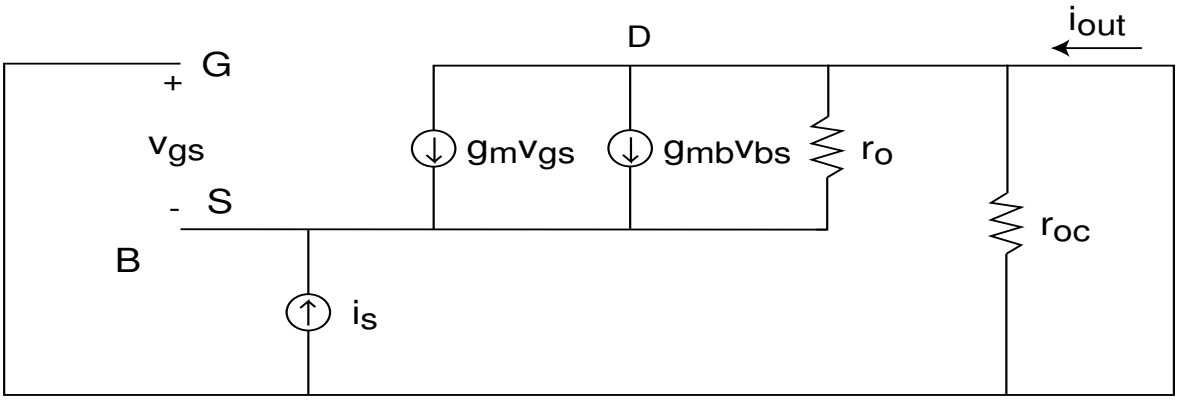
$$I_D = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2 = I_{SUP} = -I_{BIAS}$$

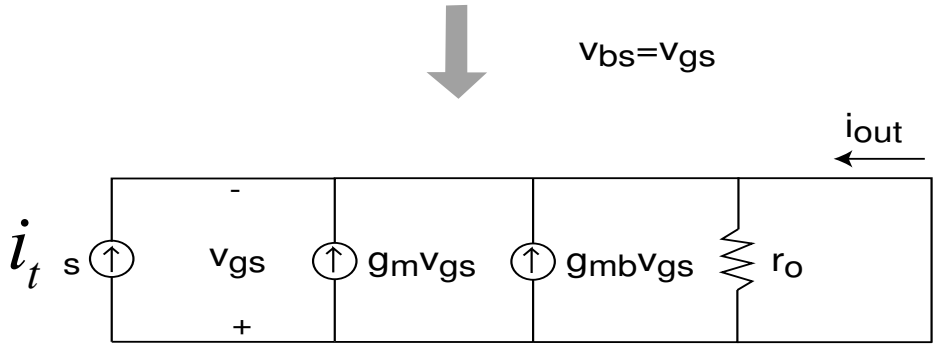
But V_T depends on V_{BS}:

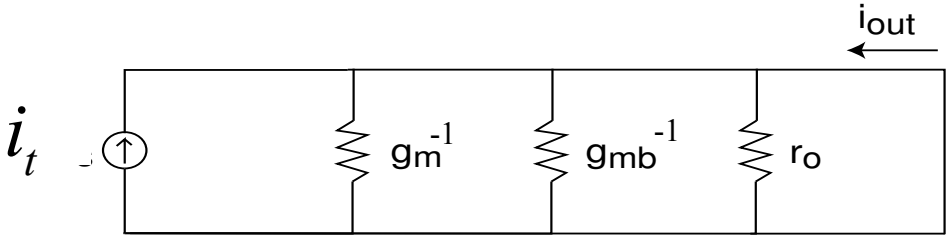
$$V_T = V_{To} + \gamma_n\left(\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p}\right)$$

Must solve these two equations iteratively.

Small-signal equivalent circuit (unloaded)





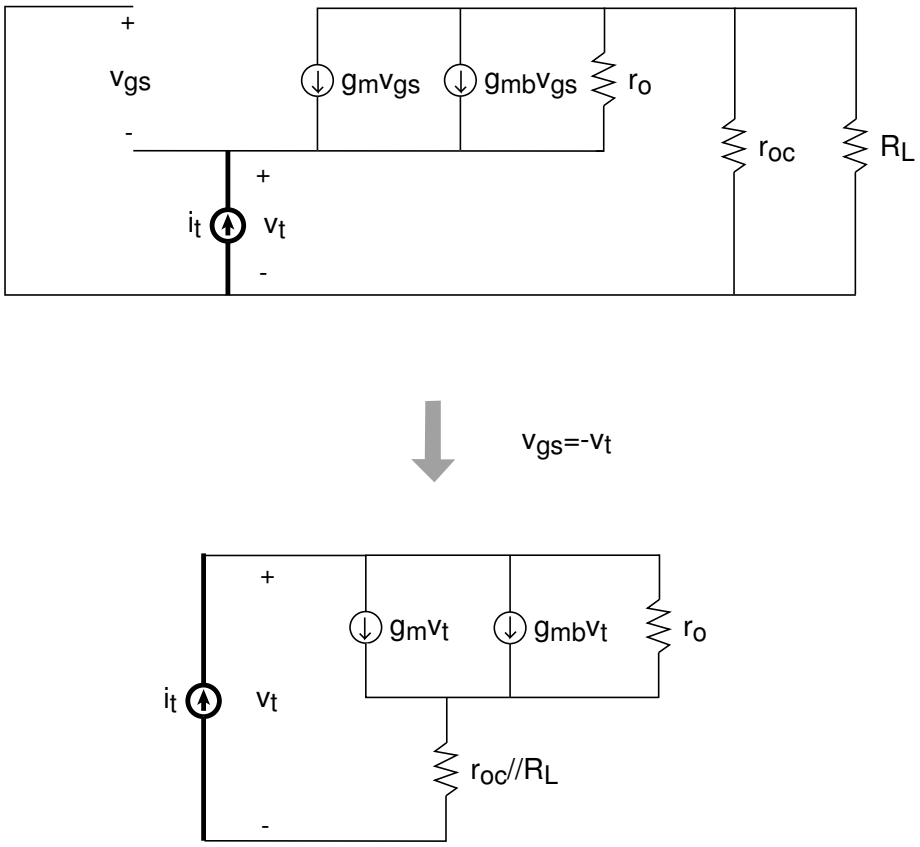


$$i_t = -i_{out} \Rightarrow A_{io} = \frac{i_{out}}{i_t} = -1$$

A_{io} is the short circuit current gain.

Not surprising, since in a MOSFET: $i_g = 0$

Input Resistance



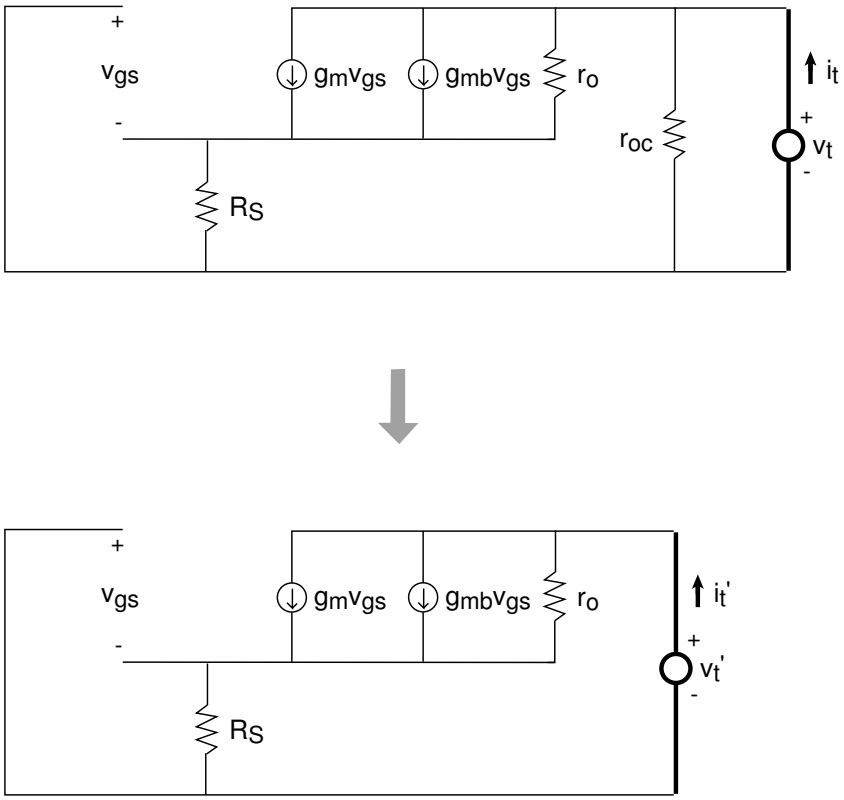
Do KCL on input node:

$$i_t - g_m v_t - g_{mb} v_t - \frac{v_t - i_t\left(r_{oc} \,//\, R_L\right)}{r_o} = 0$$

Then:

$$R_{in} = \frac{v_t}{i_t} = \frac{1 + \dfrac{r_{oc} \,//\, R_L}{r_o}}{g_m + g_{mb} + \dfrac{1}{r_o}} \approx \frac{1}{g_m + g_{mb}}$$

Output Resistance



Do KCL on input node:

$$i_t' - g_m v_{gs} - g_{mb} v_{gs} - \frac{v_t' + v_{gs}}{r_o} = 0$$

Notice also:

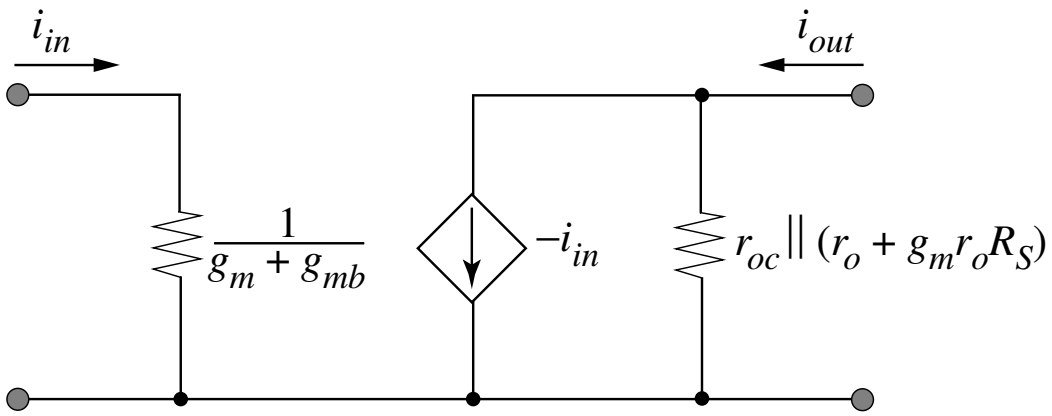
$$v_{gs} = -i_t' R_s$$

Then:

$$R_{out} = r_{oc} \,//\left(r_o \left[1 + R_s \left(g_m + g_{mb} + \frac{1}{r_o} \right) \right] \right)$$

$$R_{out} \approx r_{oc} \,//\left[r_o \left(1 + g_m R_s \right) \right] \approx r_{oc} \,//\left[\left(g_m r_o \right) R_s \right]$$

Common-Gate Two-Port Model



- The output resistance depends on the source resistance
  - The CG current buffer is not unilateral
- Input resistance << CS Amplifier
  - We want a small input resistance because the controlled generator is current controlled
- Output resistance >> CS Amplifier
  - We want a large output resistance to deliver most of the output current to the load

Relationship between circuit figures of merit and device parameters:

$$g_m = \sqrt{2 I_D \frac{W}{L} \mu_n C_{ox}}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{-2\phi_p - V_{BS}}} g_m$$

$$r_o \approx \frac{1}{\lambda_n I_D}$$

Device* Parameters	Circuit Parameters		
	$\lvert A_{io} \rvert$	R_{in}	R_{out}
	-1	$\frac{1}{g_m + g_{mb}}$	$r_{oc} // [r_o (1 + g_m R_s)]$
I_{SUP} ↑	-	↓	↓
W ↑	-	↓	↑
$\mu_n C_{ox}$ ↑	-	↓	↑
L ↑	-	↑	↑

* V_{BIAS} is adjusted so that none of the other parameters change

Common Gate amplifier is often used as a ***current buffer*** i.e. transform a current source with medium source resistance to an equal current with high source resistance (in multistage amplifiers, other stages provide the current gain).

What did we learn today?

Summary of Key Concepts

- Common-source amplifier: ***good voltage amplifier***
  better transconductance amplifier
  - Large voltage gain
  - High input resistance
  - Medium / high output resistance

- Common-drain amplifier: ***good voltage buffer***
  - Voltage gain ≈ 1
  - High input resistance
  - Low output resistance
- Common-gate amplifier: ***good current buffer***
  - Current gain ≈ 1
  - Low input resistance
  - High output resistance

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