*YOUR NAME*_____

*Department of Electrical Engineering and Computer Science*
*Massachusetts Institute of Technology*

# *6.012 Electronic Devices and Circuits*

## Exam No. 2

**Wednesday, April 16, 2008**

**7:30 to 9:30 pm**

**Notes:**

1. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.
2. Some questions ask for an explanation of your answer. No credit will be given for answers lacking this explanation.
3. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V. You should also approximate [(kT/q) ln 10] as 0.06 V.
4. Closed book; one sheet (2 pages) of notes permitted. Formula sheet provided.
5. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
6. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
7. Be careful to include the correct units with your answers when appropriate.
8. Be certain that you have all ten (10) pages of this exam booklet and the six (6) page formula sheet, and make certain that you write your name at the top of this page in the space provided.

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| 6.012 Staff Use Only | **PROBLEM 1** | _____ | (out of a possible 34) |
| | **PROBLEM 2** | _____ | (out of a possible 32) |
| | **PROBLEM 3** | _____ | (out of a possible 34) |
| | **TOTAL** | | |

**Problem 1 -** (34 points)

A collection of independent short questions in two groupings.

(a) You are in charge of a CMOS fabrication line and you have a problem because the thresholds of your n- and p-channel MOSFETs, which are supposed to be +1 V and -1 V, respectively, are turning out to be +3 V and +1 V, instead. You suspect that the interface between the silicon and the 20 nm thick oxide is contaminated with ions.

(i) [4 pts] What type of device is each transistor, enhancement mode (no channel when $v_{GS} = 0$) or depletion mode (strongly inverted when $v_{GS} = 0$)? Explain your answers.

n-channel MOSFET: _____ Depletion mode ; _____ Enhancement mode

because:

p-channel MOSFET: _____ Depletion mode; _____ Enhancement mode

because:

(ii) [4 pts] If you are right about the ions being the problem, what sign must they have, positive or negative. Explain your answer.

Ion polarity: _____ Positive; _____ Negative

because:

(iii) [4 pts] You are able to reduce the ion problem sufficiently to have the thresholds now be 1.5 V for the n-channel device and - 0.5 V for the p-channel. What impact, if any, does this remaining threshold asymmetry have on an inverter with respect to the current charging the output node, changing it from low to high, when the input goes from high to low, compared to the ideal case? Assume $V_{DD} = 3$ V. Explain.

_____ larger; _____ smaller; _____ it is similar

because:

**Problem 1 continues on the next page**

**Problem 1 continued**

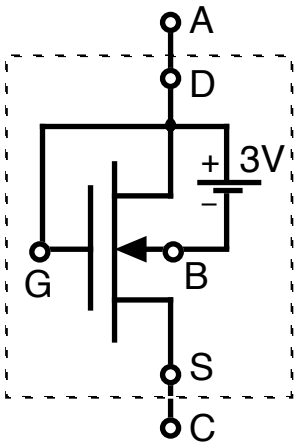
(iv) [4 pts] You are eventually able to solve the threshold asymmetry problem so that the thresholds have the same magnitude, but to do so you had to double the oxide thickness of all MOSFETs (no other dimensions were changed). What impact, if any, does this thicker oxide have on the magnitudes of the thresholds, relative to the original design? Explain.

_____ larger; _____ smaller; _____ unchanged

because

(b) These questions concern the low frequency linear equivalent circuits of MOSFETs.

(i) [6 pts] Consider the n-channel MOSFET circuit pictured to the right. The circuit is biased with $V_{AC}$ = 2 Volts. The MOSFET has following parameters:




$K = 2\ mA/V^2$
$V_T = 1\ V$
$\alpha = 1$
$\lambda = 0.01\ V^{-1}$
$\eta = 0.2$

A small signal voltage, $v_{ac}(t)$, is added to the 2 V bias so now $v_{AC}(t) = 2\ V + v_{ac}(t)$. First find the bias and small signal values of $v_{GS}$, $v_{DS}$, and $v_{BS}$, and then draw a single element small signal linear equivalent circuit for this connection and give an expression for this element in terms of $g_m$ and $g_o$.

$V_{GS}$:_____ $V_{BS}$:_____ $V_{DS}$:_____

$v_{gs}$:_____ $v_{ds}$:_____ $v_{bs}$:_____

Linear equivalent circuit:

Element: _____ = _____

**Problem 1 continues on the next page**

**Problem 1 continued**

(ii) [3 pts] Consider two MOSFETs, one an n-channel MOSFET and the other a p-channel MOSFET. They have identical dimensions, and both are biased in saturation at the same drain current, $|I_D|$. Which of the devices, if either, would have the larger transconductance, $g_m$, and why?

_____ n-channel; _____ p-channel; _____ they are similar

because:

(iii) [3 pts] Consider two MOSFETs, one an n-channel MOSFET and the other a p-channel MOSFET. They have identical dimensions, and both are biased in sub-threshold at the same drain current, $|I_D|$. Which of the devices, if either, would have the larger transconductance, $g_m$, and why?

_____ n-channel; _____ p-channel; _____ they are similar

because:

(iv) [6 pts] An n-channel MOSFET in a circuit was mistakenly biased in its linear region. Derive expressions in terms of $V_{GS}$, $V_{DS}$, and K for its transconductance, $g_m$, and output conductance, $g_o$, in this situation. Assume $v_{BS} = 0$ and $\alpha = 1$, and ignore the Early effect, i.e., assume $\lambda = 0$.

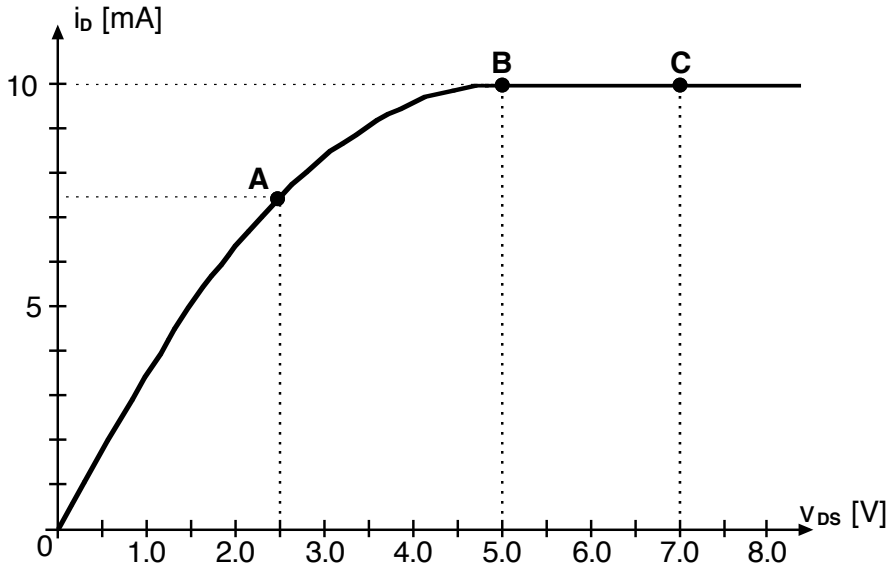
Transconductance, $g_m$ = _____

Output conductance, $g_o$ = _____

**End of Problem 1**

**Problem 2 -** (32 points)

The $I_D$-$V_{DS}$ plot for an ideal n-channel MOSFET ($\alpha$=1) is shown below. The substrate bias, $V_{BS}$, is 0 V, the saturation current, $I_{Dsat}$, is 10 mA, and the saturation voltage, $V_{DS,sat}$, is 5 V. For this device $t_{ox}$=10 nm, $\varepsilon_{ox}$= 3.5 x $10^{-13}$ F/cm, W= 50 μm, and L=10 μm.




(a) [4 pts] Given that $V_T$ = 1 V, what is the gate voltage $V_{GS}$ that must be applied to obtain the characteristic shown above?

$V_{GS}$ = _____ Volts

(b) [5 pts] What is the slope, $di_D/dv_{DS}$ of the characteristic at $V_{DS}$ = 0V? Make sure you provide a formula as well as a value so that your answer is independent of the correctness of your Part (a).

$di_D/dv_{DS}$ @ $V_{DS}$ = 0: Formula_____

Value_____ S

**Problem 2 continues on the next page**

**Problem 2 continued**

(c) [8 pts] Since $\alpha$=1 you can assume that $V_T$ is independent of position in the channel. With this assumption in mind calculate the inversion layer sheet charge density, $q_N^*(y)$ corresponding to Bias Point A (i) adjacent to the source (the source end, y = 0) and (ii) adjacent to the drain (drain end, y = L).

(i) $q_N^*(0)$ at source end for Bias Point A: _____ Coul/cm$^2$

(ii) $q_N^*(L)$ at drain end for Bias Point A: _____ Coul/cm$^2$

(d) [6 pts] Calculate the electron drift velocity, $s_{e\text{-}Drift}$, at the (i) source end and (ii) drain end of the channel at Bias Point A. If you could not solve Part (c) express your answers in terms of the appropriate $q_N^*$.

(i) $s_{e\text{-}Drift}$ at source end, y = 0, for Bias Point A: _____ cm/s

(ii) $s_{e\text{-}Drift}$ at drain end, y = L, for Bias Point A: _____ cm/s

(e) [6 pts] The transistor enters saturation at Bias Point B and simple theory suggests that the drain-end charge has become 0 while the drain-end velocity is infinite, so that the $I_{DSat}$ can flow in that part. Now, assuming instead that the electrons at the drain end move at their saturation velocity, $s_{sat}=10^7$ cm/s, what is the channel charge density that must exist there to support the $I_{Dsat}$?

$q_N^*(L)$ at drain end in saturation, Bias Pts B and C: _____ Coul/cm$^2$

**Problem 2 continues on the next page**

**Problem 2 continued**

(f) [3 pts] Assuming $V_{CS}(y)$ is the voltage that a hypothetical voltmeter would measure between the inversion layer at position y along the channel and the source. Derive an expression that could be solved for $V_{CS}(L/2)$, i.e. at distance $L/2$ from the source in a device biased at Bias Point C, in terms of the transistor parameters and $I_{Dsat}$. You <u>do not</u> have to solve the expression to obtain a numerical value for $V_{CS}$; your expression can be an integral or differential equation. Assume there is no velocity saturation.

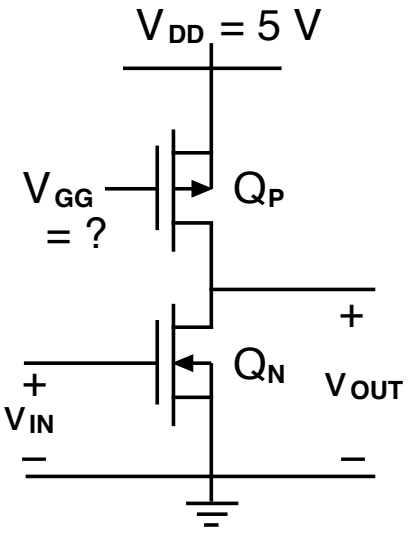
NOTE: Do not spend a lot of time on this sub-question. If you don't see what to do right away, move on and come back to try again later if you have time.

$V_{CS}$ @ $y = L/2$ at Bias Pt. C: Expression_____

**End of Problem 2**

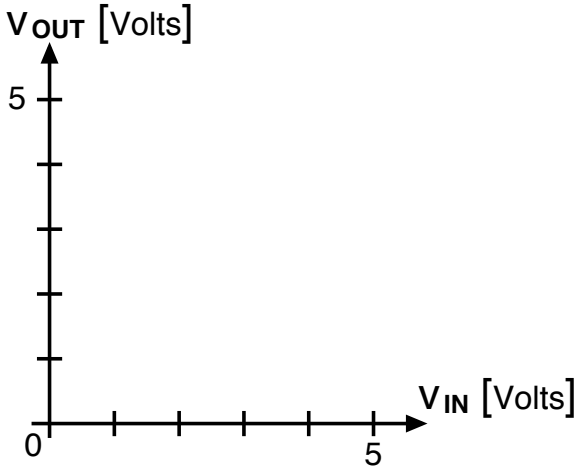
**Problem 3** (34 points)

This problem analyzes the inverter shown below. The parameters for the n-channel MOSFET pull-down transistor, and the p-channel MOSFET pull-up transistor are given below the figure. The value of the supply voltage $V_{GG}$ is not specified (you will find it in Part c), but you can assume that its value is such that $Q_P$ is not cut-off.

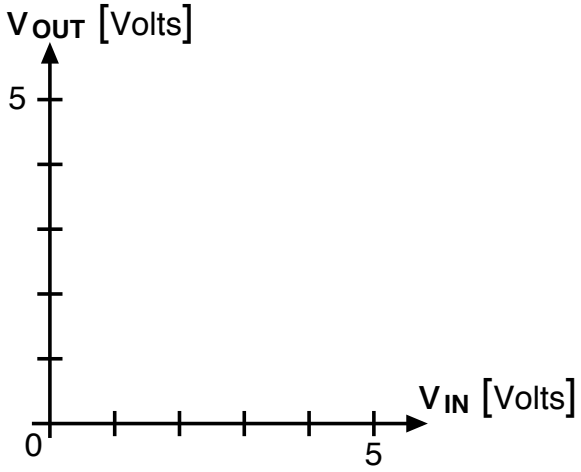



Parameters for the n-channel MOSFET ($Q_N$) and p-channel MOSFET ($Q_P$):
$L_N = L_P = 1\ \mu m$; $W_N = 10\ \mu m$, $W_P = 25\ \mu m$; $\mu_e = 500\ cm^2/V\text{-}s$, $\mu_h = 200\ cm^2/V\text{-}s$;
$V_{TN} = 1\ V$, $V_{TP} = -1\ V$; $C^*_{ox} = 6 \times 10^{-7}\ F/cm^2$; $\lambda_N = \lambda_P = 0.1\ V^{-1}$; $n_N = n_P = 1.5$.

(a) [4 pts] On the two sets of axes provided below, indicate the regions in $v_{IN}$-$v_{OUT}$ space where each device is off, linear, and saturated.




(i) n-channel MOSFET, $Q_N$

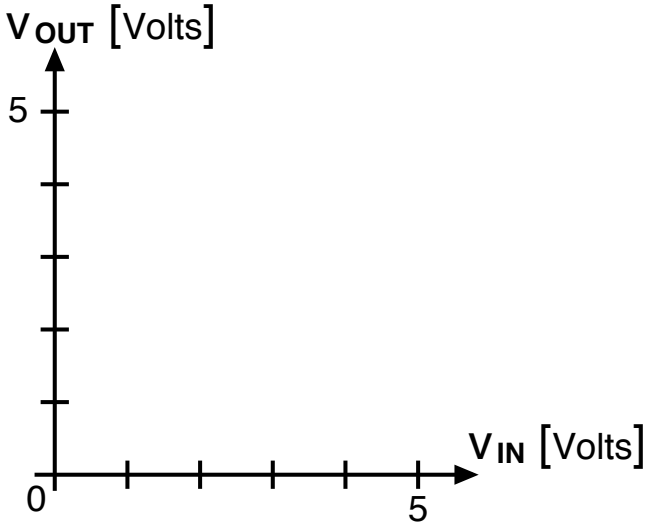



(ii) p-channel MOSFET, $Q_P$

**Problem 3 continues on the next page**

**Problem 3 continued**

(b) [5 pts] Assuming that this inverter is designed such that $V_M = V_{IN} = V_{OUT} = V_{DD}/2$ sketch the transfer characteristic, $V_{OUT}$ vs. $V_{IN}$, on the set of axes provided below. Identify on this sketch the regions of operation of the two MOSFETs. This should be a "free-hand" sketch without paying close attention to the parameters of the MOSFETs.




(c) [4 pts] Determine what value the pull-up gate bias voltage, $V_{GG}$, must have to make the logic threshold $V_M = V_{IN} = V_{OUT} = V_{DD}/2$. If you could not do Parts (a) and (b) you may assume both transistors are in saturation at this point. ***Ignore channel length modulation.*** (Note: $V_M$ is the point on the transfer characteristic where $v_{IN} = v_{OUT}$.)

$V_{GG}$ = _____ Volts

(d) [6 pts] If $V_M = V_{DD}/2$, determine the voltage gain $A_V(V_M)$ at the bias point $V_{IN} = V_{OUT} = V_M = V_{DD}/2$. If you could not do Parts (a) and (c) you may assume both transistors are in saturation at this point. ***You must include channel length modulation in your analysis for this question.***

$A_v(V_M)$ = _____

**Problem 3 continues on the next page**

**Problem 3 continued**

(e) [5 pts] What is the static power dissipation, $P_{Static}$, of this gate when $V_{IN} = 5$ V?

$P_{Static}$ when $V_{IN} = 5$ V: _____ W

(f) [5 pts] What is the static power dissipation, $P_{Static}$, of this gate when $V_{IN} = 0$ V?

$P_{Static}$ when $V_{IN} = 0$ V: _____ W

(g) [5 pts] Assuming that $W_n/L_n = 10$, $W_p/L_p = 25$, and $V_{GG} = 2.5$ V, what is the propagation delay for the low to high output transition, $\tau_{Lo\text{-}Hi}$, if the inverter is driving a capacitive load of 100 fF?

$\tau_{Lo\text{-}Hi}$ = _____ s

**End of Problem 3**

**End of Exam Two**

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