May 24, 2001 - Final Exam

problem	grade
1	
2	
3	
4	
5	
total	

Name: ______________________________

Recitation: ______________________________

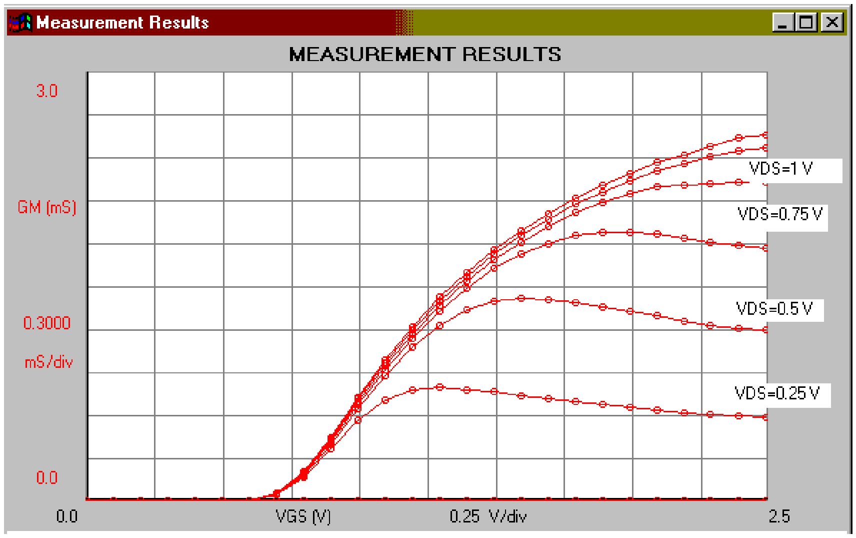
General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back page.
- You have **180 minutes** to complete your exam.
- Unless stated otherwise, assume room temperature.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, E, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use $\phi = 0$ at $n_o = p_o = n_i$ as potential reference.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$$n_i = 1 \times 10^{10}\ cm^{-3}$$
$$kT/q = 0.025\ V$$
$$q = 1.60 \times 10^{-19}\ C$$
$$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$$
$$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$$

1. *(15 points)* The figure below shows the measured transconductance characteristics of the n-channel MOSFET that you characterized in *Device Characterization Project #2*. Each of the lines represents a different value of V_{DS}, starting with $V_{DS,min} = 0.25\ V$, in steps of $\Delta V_{DS} = 0.25\ V$.

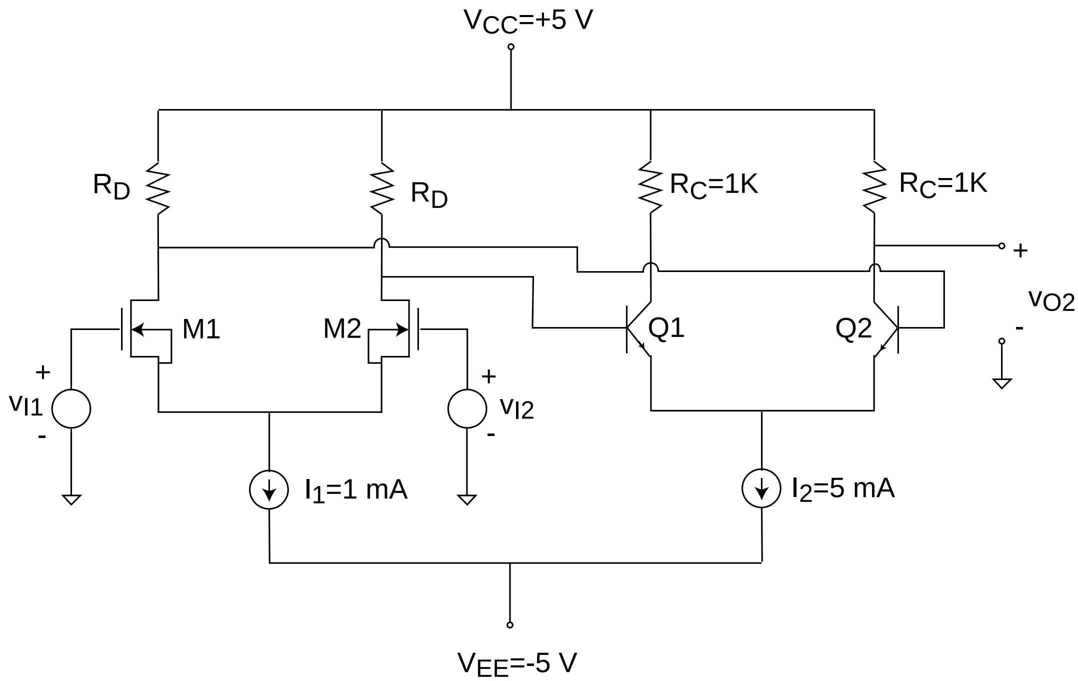
This device has $L = 1.5\ \mu m$ and $W = 46.5\ \mu m$.



(1a) *(10 points)* In the space below, carefully sketch the g_m vs. V_{GS} characteristics predicted by the *ideal* MOSFET model presented in 6.012. Indicate the evolution of g_m for several values of V_{DS}. Derive suitable equations for each of the branches that you identify.

(1b) *(5 points)* From the data shown in the figure above, estimate V_T and $\mu_n C_{ox}$ for the measured device.

2. *(15 points)* Consider the two-stage BiCMOS differential amplifier below.



M1 and M2 are identical and are biased in the saturation regime. Q1 and Q2 are also identical and are biased in the forward active regime. Suitable parameters for these transistors are:

nMOSFET: $V_T = 1\ V$ and $\frac{W}{L}\mu_n C_{ox} = 0.1\ mA/V^2$

npn BJT: $\beta_F = 250$, $V_{BEon} = 0.7\ V$ and $V_{CEsat} = 0.2\ V$

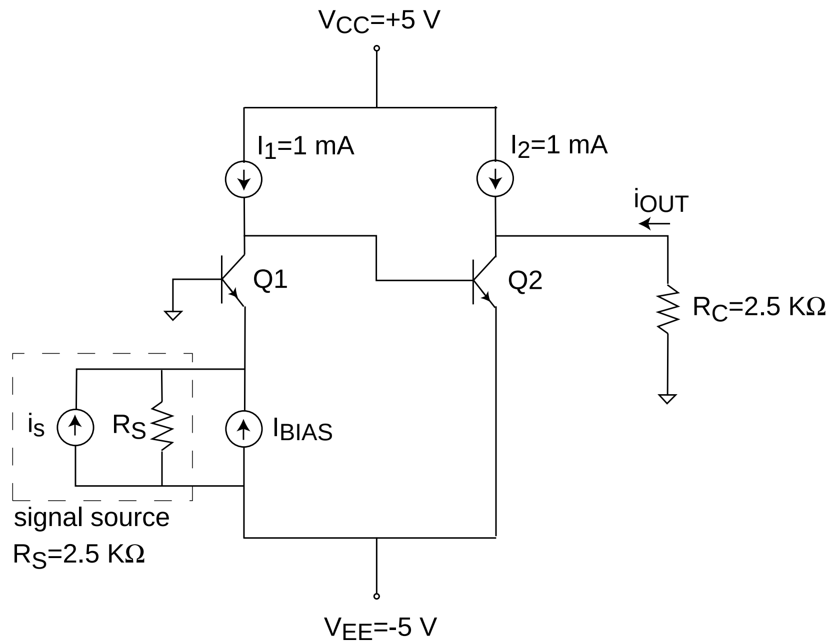
The current sources I_1 and I_2 need at least $0.5\ V$ across to operate properly.

(2a) *(5 points)* Compute the power dissipation of this amplifier.

(2b) *(5 points)* What constraint is imposed on R_D so that the amplifier can properly handle a *maximum common-mode input* of 3 V? (Express your answer as $R_D > X$ *or* $R_D < X$. Give value of X).

(2c) *(5 points)* If $R_D = 5\ k\Omega$, what is the maximum possible voltage swing of node V_{O2} with respect to ground? Give V_{O2min} and V_{O2max}.

3. *(25 points)* Consider the two-stage bipolar current amplifier shown below. At the input of this amplifier there is a signal source with an internal resistance $R_S = 2.5\ k\Omega$; at the output, there is a load characterized by $R_L = 2.5\ k\Omega$.



Both transistors in this amplifier are identical and are characterized by the following parameters: $\beta_F = 100$ and $V_A = 50\ V$. Treat all biasing current sources as ideal, that is, with infinite internal resistance.

(3a) *(10 points)* Draw a two-port low-frequency small-signal equivalent-circuit model of the first stage of this amplifier. Derive values for all elements of this two-port model.

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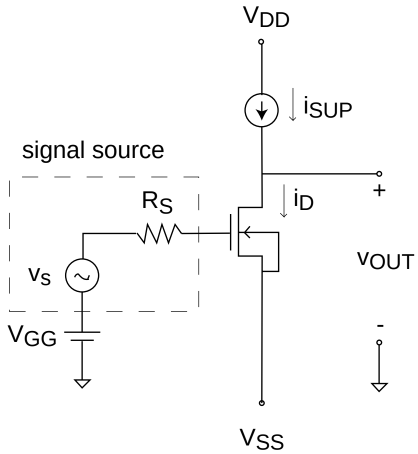
(3b) *(10 points)* Draw a two-port low-frequency small-signal equivalent-circuit model of the second stage of this amplifier. Derive values for all elements of this two-port model.

(3c) *(5 points)* Calculate the *loaded current gain* $A_i = \frac{i_{out}}{i_s}$ of this amplifier.

4. *(15 points)* The diagram below shows an *unloaded* common-source amplifier with a current source supply. The adjoining table describes the relationship between device parameters and circuit parameters for this amplifier stage.



Device * Parameters	Circuit Parameters $\lvert A_{vo}\rvert$	R_{in}	R_{out}	ω_H
$I_{SUP} \uparrow$	$\downarrow$	-	$\downarrow$	
$W \uparrow$	$\uparrow$	-	-	
$\mu_n C_{ox} \uparrow$	$\uparrow$	-	-	
$L \uparrow$	$\uparrow$	-	$\uparrow$	

In this table, when changing one of the device parameters, adjustments are made to V_{GG}, the gate bias, so that none of the other parameters are affected.

In this problem, you have to fill the fourth column of this table that contains the 3dB bandwidth of the amplifier. Use the same format as in the rest of the table and indicate in what direction ω_H will change when the device parameters increase one at a time. Nothing else changes, except perhaps for V_{GG} as explained above. In the space below, provide an explanation for your entry. *If there is no explanation, there are no points!*

(4a) *(3 points)* If $I_{SUP} \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, $\downarrow$. Why?

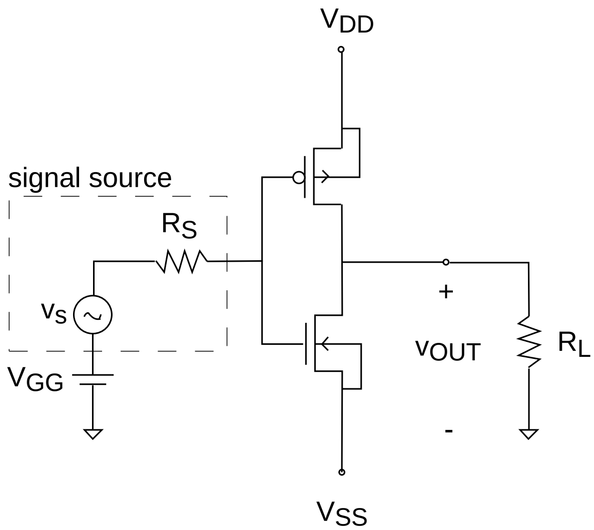
(4b) *(3 points)* If $W \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, $\downarrow$. Why?

(4c) *(3 points)* If $\mu_n C_{ox} \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, $\downarrow$. Why?

(4d) *(3 points)* If $L \uparrow$, how does ω_H change? Select: $\uparrow$, $-$, $\downarrow$. Why?

(4e) *(3 points)* If we now connect the output of the amplifier to a load resistance $R_L \ll r_o//r_{oc}$, how does ω_H change? Select: $\uparrow$, $-$, $\downarrow$. Why?

5. *(30 points)* Consider the following CMOS amplifier:



The devices are characterized by the following parameters:

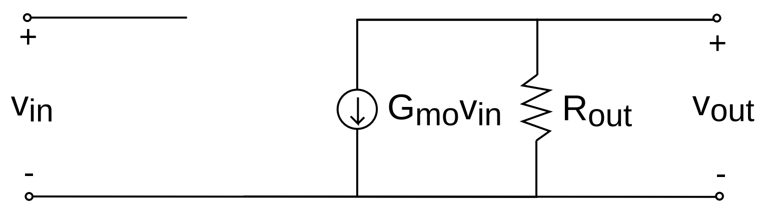
nMOS: $L_n = 1\ \mu m$, $W_n = 4\ \mu m$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{Tn} = 1\ V$, $\lambda_n = 0.1\ V^{-1}$, $C_{gsn} = 6\ fF$, $C_{gdn} = 1\ fF$, $C_{dbn} = 5\ fF$.

pMOS: $L_p = 1\ \mu m$, $W_p = 8\ \mu m$, $\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{Tp} = -1\ V$, $\lambda_p = 0.1\ V^{-1}$, $C_{gsp} = 12\ fF$, $C_{gdp} = 2\ fF$, $C_{dbp} = 10\ fF$.

Other values are: $V_{DD} = 5\ V$, $V_{SS} = -5\ V$, $R_S = 1\ k\Omega$, and $R_L = 1\ k\Omega$.

(5a) *(5 points)* Compute the value of V_{GG} required to obtain a quiescent output voltage $V_{OUT} = 0\ V$.

A low-frequency small-signal equivalent circuit model for this amplifier in an *unloaded* configuration at the bias point specified in part (5a) is given below:



with $G_{mo} = 1.6\ mS$ and $R_{out} = 3.1\ k\Omega$.

(5b) *(5 points)* Calculate the *loaded* voltage gain of the entire CMOS amplifier (don't be alarmed if it comes out a bit small, this is not a very good amplifier).

(5c) *(15 points)* Estimate the 3 dB bandwidth of the entire CMOS amplifier (that is, in its loaded configuration). To do this, calculate the time constant of each capacitor at a time *(six capacitors at 2 points each)*. Then compute the 3 dB bandwidth in *Hz (3 points)*.

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(5d) *(5 points)* Calculate the voltage swing of the output node of this amplifier in its loaded confi-turation.