

MITOCW | MIT6_004S17_20-02-05_300k

Serial point-to-point links are the modern replacement for the parallel communications bus with all its electrical and timing issues. Each link is unidirectional and has only a single driver and the receiver recovers the clock signal from the data stream, so there are no complications from sharing the channel, clock skew, and electrical problems.

The very controlled electrical environment enables very high signaling rates, well up into the gigahertz range using today's technologies.

If more throughput is needed, you can use multiple serial links in parallel.

Extra logic is needed to reassemble the original data from multiple packets sent in parallel over multiple links, but the cost of the required logic gates is very modest in current technologies.

Note that the expansion strategy of modern systems still uses the notion of an add-in card that plugs into the motherboard.

But instead of connecting to a parallel bus, the add-in card connects to one or more point-to-point communication links.

Here's the system-level communications diagram for a recent system based on an Intel Core i7 CPU chip.

The CPU is connected directly to the memories for the highest-possible memory bandwidth,

but talks to all the other components over the QuickPath Interconnect (QPI), which has 20 differential signaling paths in each direction.

QPI supports up to 6.4 billion 20-bit transfers in each direction every second.

All the other communication channels (USB, PCIe, networks, Serial ATA, Audio, etc.) are also serial links, providing various communication bandwidths depending on the application.

Reading about the QPI channel used by the CPU reminded me a lot of the one ring that could be used to control all of Middle Earth in the Tolkien trilogy Lord of the Rings.

Why mess around with a lot of specialized communication channels when you have a single solution that's powerful enough to solve all your communication needs?

PCI Express (PCIe) is often used as the communication link between components on the system motherboard.

A single PCIe version 2 "lane" transmits data at 5 Gb/sec using low-voltage differential signaling (LVDS) over wires designed to have a 100-Ohm characteristic impedance.

The PCIe lane is under the control of the same sort of network stack as described earlier.

The physical layer transmits packet data through the wire.

Each packet starts with a training sequence to synchronize the receiver's clock-recovery circuitry, followed by a unique start sequence, then the packet's data payload, and ends with a unique end sequence.

The physical layer payload is organized as a sequence number, a transaction-layer payload and a cyclical redundancy check sequence that's used to validate the data.

Using the sequence number, the data link layer can tell when a packet has been dropped and request the transmitter restart transmission at the missing packet.

It also deals with flow control issues.

Finally, the transaction layer reassembles the message from the transaction layer payloads from all the lanes and uses the header to identify the intended recipient at the receive end.

Altogether, a significant amount of logic is needed to send and receive messages on multiple PCIe lanes, but the cost is quite acceptable when using today's integrated circuit technologies.

Using 8 lanes, the maximum transfer rate is 4 GB/sec, capable of satisfying the needs of high-performance peripherals such as graphics cards.

So knowledge from the networking world has reshaped how components communicate on the motherboard, driving the transition from parallel buses to a handful of serial point-to-point links.

As a result today's systems are faster, more reliable, more energy-efficient and smaller than ever before.